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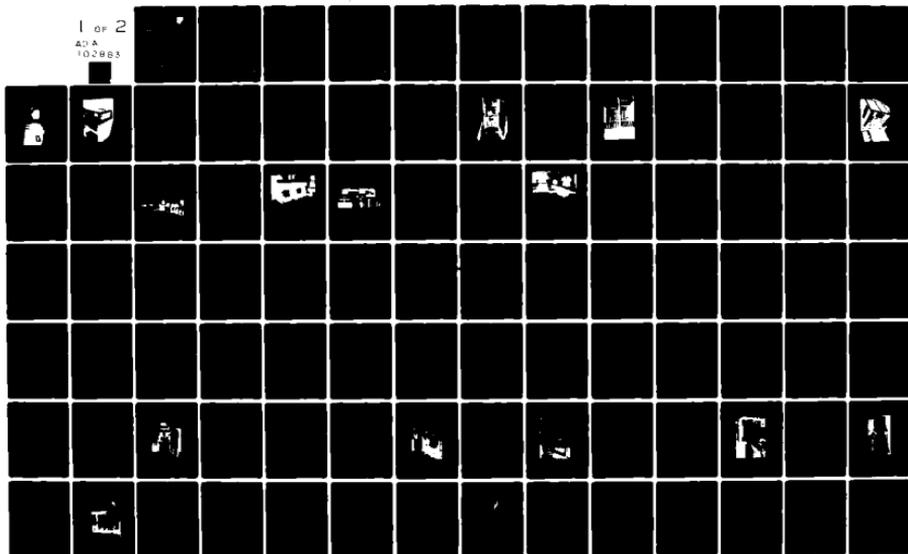
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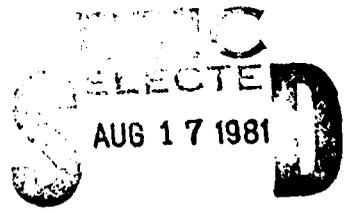


TACTICAL OPERATIONS ANALYSIS SUPPORT FACILITY

TRW/Defense and Space Systems Group

M. P. Murphey
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This report describes, in detail, the current computer hardware and operating system software configuration of the Tactical Operations Analysis Support (TOAS) Facility, at Langley AFB VA . The TOAS is the focal point for test and demonstration activities sponsored by the RADC Project 2315, Automated Tactical Intelligence. Project 2315 is directed at developing new and improved automation techniques and procedures to enhance Tactical Operational Intelligence support. This report pro-			

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1. INTRODUCTION

The Tactical Operations Analysis Support (TOAS) Facility is an advanced development effort sponsored by the Rome Air Development Center (RADC) as part of Project 2315 - Automated Tactical Intelligence. The primary objective of the TOAS Facility effort is to provide a computer hardware and software environment to support the automation demonstrations and experiments of the other Project 2315 contractors and government agencies. The final goal of Project 2315 is to provide the design specifications for an automated Tactical Air Intelligence System (TAIS) to support tactical Air Force operations in the 1990 timeframe.

1.1 TACTICAL OPERATIONS ANALYSIS SUPPORT (TOAS) FACILITY

A direct approach was used to implement the TOAS Facility requirement for automated R&D tools for developing, evaluating, and testing

- Software systems,
- Hardware Components, and
- Functional Procedures.

The Facility was located at Langley Air Force Base, Virginia, in order that the Air Force user could readily be a major participant in the R&D process. This close user-developer relationship provides better functional requirement definition and valuable user comment/guidance for on-going R&D efforts.

The current Facility configuration consists of two DEC PDP-11/70 computers, DEC system peripherals, and graphics display devices (SU 1652 and Imlac PDS-4). A Bunker Ramo multiplexer is also available. As new hardware and baseline system software needs are evolved, the Facility computer environment will be changed to support the new requirements. This document provides a technical description of the baseline computer resources, the management and maintenance procedures, and technology issues for investigation at the TOAS Facility.

1.2 TOAS FACILITY TECHNICAL REPORT

The purpose of this interim report is to update and expand the TOAS Baseline Interim Technical Report dated February 1980. Section 2 is a technical description of the TOAS hardware and software modules that currently compose the baseline configuration. The purpose of this section is to insure the basic technical system specifications and capabilities are available to companies/agencies who will be using the TOAS Facility for software development and demonstration. Section 3 is the TOAS Facility Management Plan. This Plan details the TOAS Facility operating procedures/practices and establishes Facility management responsibilities and system configuration guidelines. Section 4 documents the hardware preventive maintenance inspection (PMI) tasks, diagnostic requirements, and corrective maintenance procedures for the Facility hardware. These procedures will be used to determine the operational status of TOAS hardware components. Section 5 is an overview of several technologies that were not included in the baseline configuration and proposes equipment for future testing/demonstration at the TOAS facility.

2. BASELINE SYSTEM DESCRIPTION

This section provides the current TOAS Facility configuration and technical descriptions of the hardware and system software resources. Project 2315 and other Air Force sponsored R&D projects will use this facility to test and demonstrate software developed using compatible computer hardware configurations. In order to minimize software conversion and installation time at the TOAS Facility, software demonstration sponsors should be familiar with the overall TOAS system configuration and resource technical descriptions to determine areas that may adversely impact on the planned demonstration. If required, additional technical data is available from the on-site TRW representatives and the manufacturer's technical documentation available at the TOAS facility.

2.1 SYSTEM CONFIGURATION

The TOAS Facility consists of a dual PDP 11/70 computers, system support peripherals, and various user interface devices. The computers are currently operating in autonomous modes to support a dedicated system (System A) for specific functional demonstration/experimentation work and a software development timesharing system (System B). The overall system block diagram is provided in Figure 2-1. Facility hardware components are listed in Table 2-1. System B is shown in Figure 2-2.

2.2 HARDWARE TECHNICAL DESCRIPTION

The major features of the hardware are documented herein for ready reference, and to aid in comprehending the technical aspects of the TOAS Facility hardware.

2.2.1 Central Processing Unit

The PDP-11/70 Central Processing Unit (CPU) is a 16 bit processor for high-speed, real time applications, and for large multi-user, multi-task, time shared applications requiring large amounts of addressable memory. Figure 2-3 depicts the CPU boards and the operator's console.

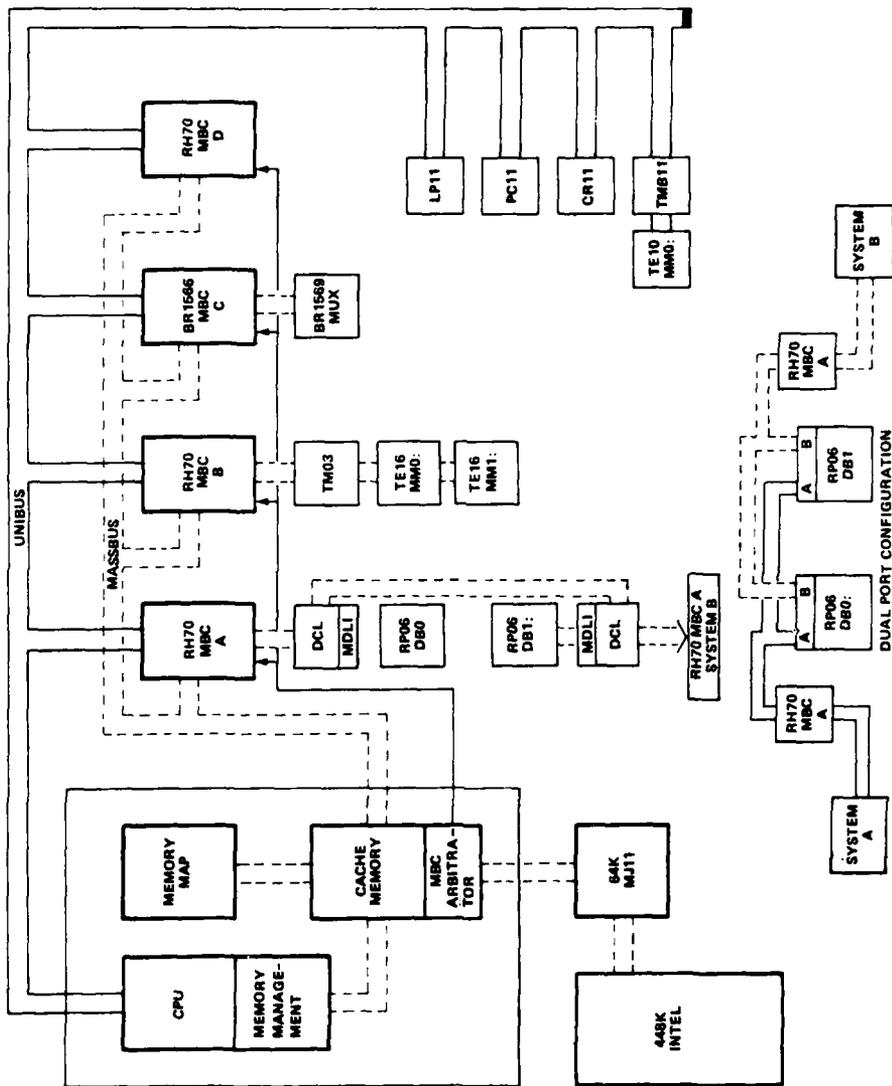


Figure 2-1. System A Block Diagram

Table 2-1 TOAS Hardware List

Manufacturer	Model	Description	Quantity
<u>DEC</u>	PDP-11/70	Computer CPU, 128K core	2
	FP-11C	Floating Point Processor	2
	KW-11P	Programmable Real-time clock	2
	RWP-06BA	Dual Access Disk Controller	2
	RP-06	Dual Access Disk Drive	2
	TWE-16EA	9 Track Tape Controller/Drive	2
	TE-16EE	9 Track Tape Drives	2
	TME-11EA	7 Track Tape Drive	2
	LP-11VA	300 lpm Printer	2
	CR-11	300 cpm Card Reader	2
	PC-11	Paper Tape Punch/Reader	2
	DMC-11AR	DDCMP Micro Processor	2
	DMC-11DA	Network Link Line Unit	2
	DL-11E	Async Serial Line Interface	4
<u>Intel</u>	IN-1670	448K Words MOS Memory	2
<u>Univac</u>	SU-1652	Dual Screen Monitor	2
<u>Imlac</u>	PDS-4	Graphic Display System	2
<u>Bunker Ramo</u>	BR-1569	8 Channel Multiplexer	1

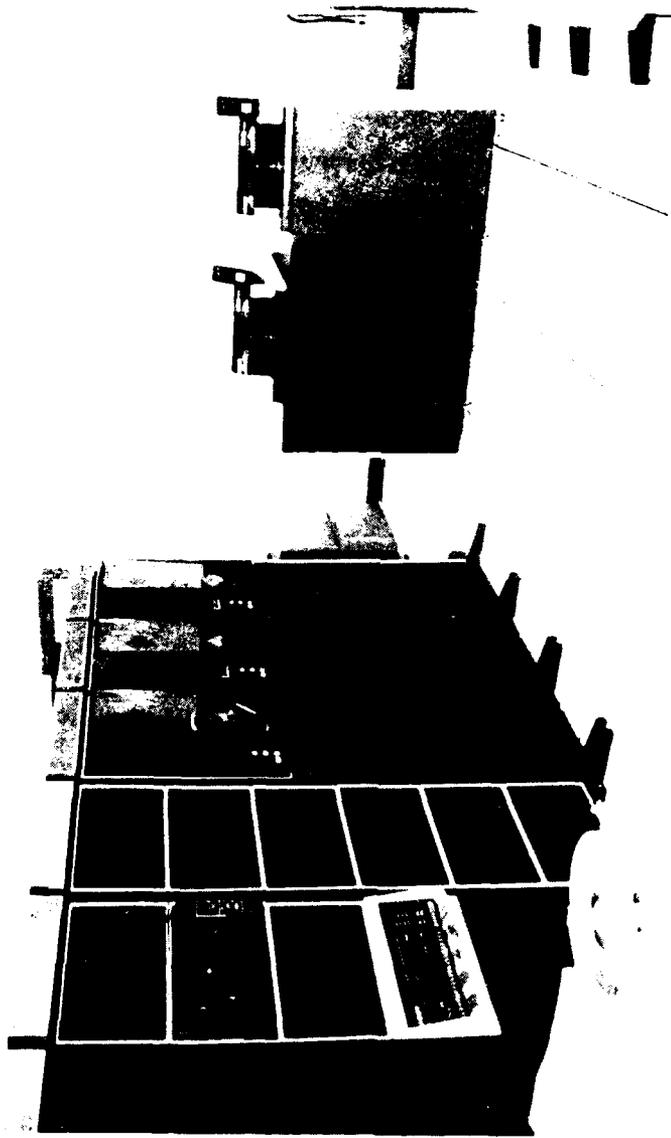


Figure 2-2. TOAS Facility Computer System B

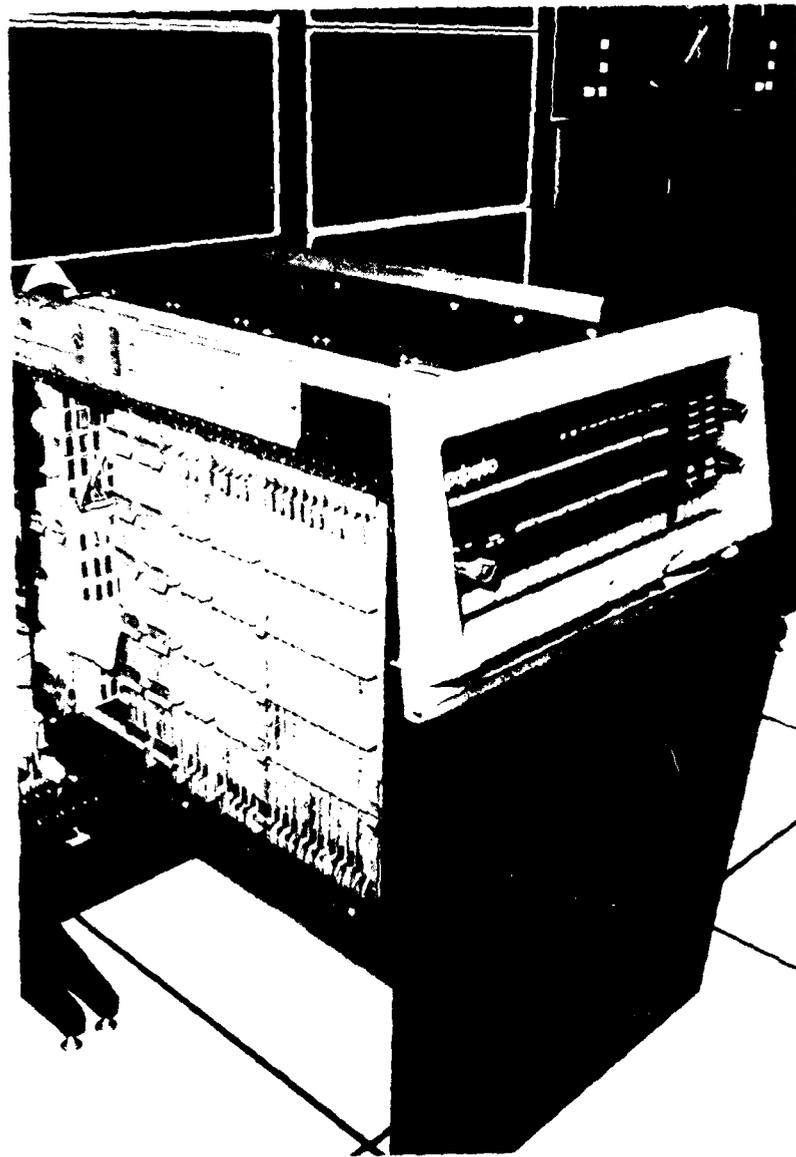


Figure 2-3. PDP-11/70 CPU and Console

Integral components of the CPU include: Cache Memory organization to provide a high-speed memory; 32-bit internal data paths with parity; floating-point processor; Memory Management for relocation and protection in multi-user, multi-task environments; access to 64K words of MJ11-A core memory and 448K words of Intel semi-conductor memory; and high-speed mass buss I/O controllers. The CPU organization for System A and System B is given in Figure 2-4.

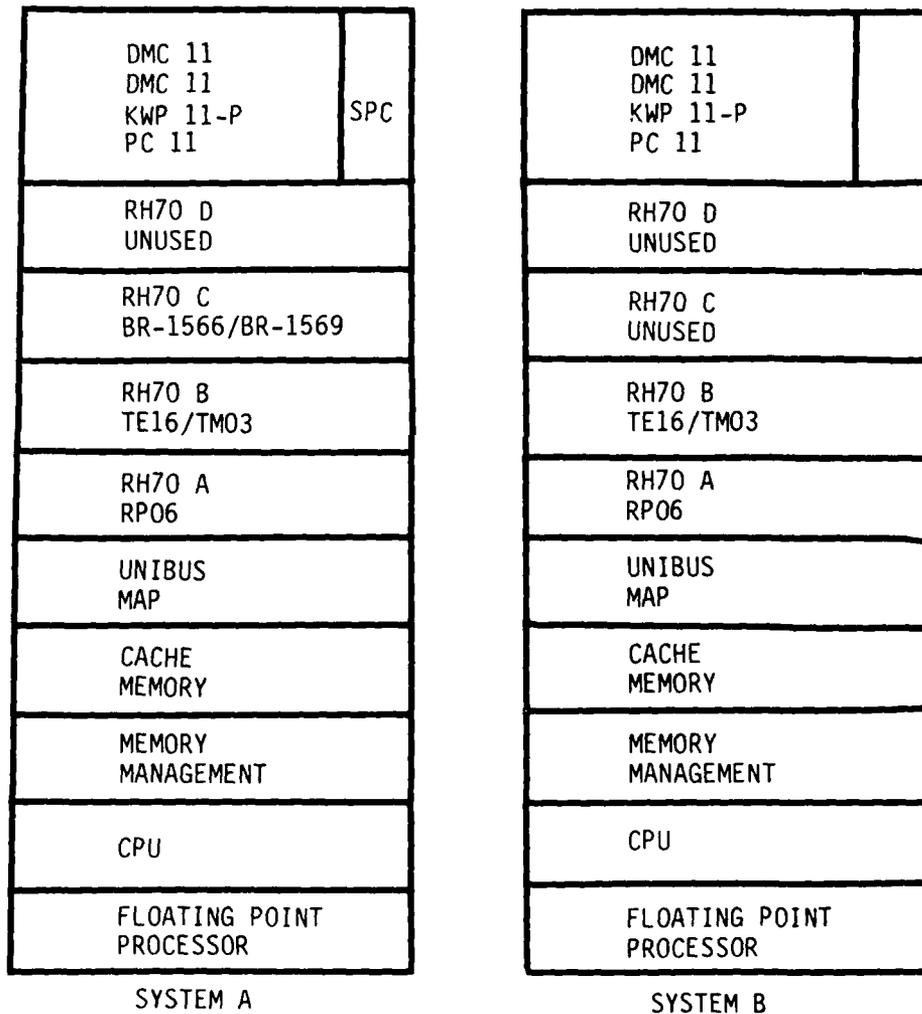


Figure 2-4. CPU Organization

2.2.1.1 KWB11-C Processor

The processor is the instruction execution section of the system, implementing an extended version of the PDP-11/45 instruction set. It contains arithmetic and control logic for a wide range of operations including high-speed floating-point and integer arithmetic with hardware multiply and divide. The KWB11-C also contains 16 general registers, variable stack overflow, 4-level vectored priority interrupts, extensive test and branch operations, and acts as an arbitrating unit for Unibus control.

2.2.1.2 FP11-C Floating-Point Processor

The FP11-C Floating-Point Processor (FPP) is a hardware option utilized by the PDP-11/70 that enables the CPU to perform arithmetic and logic operations using floating-point arithmetic. The prime advantage is increased speed without need of writing complex floating-point software routines.

The FP11-C is connected directly to the CPU and not the Unibus. This allows addressing of floating-point memory references which utilizes the Memory Management option. Floating-point instructions can reference any memory location, the CPU general registers, and any of the floating-point accumulators. Some notable features of the FP11-C are listed below.

- Performs arithmetic operations on single-precision (32-bit) and double-precision (64-bit) numbers. Both numbers have 8 bits of exponent and one sign bit; the 32-bit number contains 23-bits of fraction and the 64-bit number contains 55-bits of fraction.
- Includes special instructions to optimize I/O routines and mathematical sub-routines.
- Capable of converting 16- or 32-bit integers to 32- or 64-bit floating-point numbers and vice versa. Also is capable of converting single-precision floating-point to double precision floating-point and vice versa.
- High floating-point throughput with built-in maintenance instructions for ease of maintenance.

The FP11-C depends on the CPU to fetch instructions and data; control of the program resides in the CPU, therefore the CPU must initiate floating-point operations and supply addresses/data as required.

If the CPU fetches an instruction from memory that is not a floating-point instruction, the FP11-C ignores the instruction. If it is a floating-point instruction, it contains a floating-point designated op-code and the CPU branches to the CPU ROM states associated with floating-point instructions.

2.2.1.3 Cache Memory

Cache memory is a 1K word bi-polar MOS high-speed memory that acts as an interface buffer between the CPU registers and Main memory. The Cache is completely transparent to all programs. Programs are treated as if there were one continuous memory.

Whenever a request is made by the CPU to fetch data from memory, the Cache does an address compare to see if it contains the address of the data requested. If the Cache contains the address of the data, the data is fetched and a Main memory read is not required. A Cache to CPU data transfer takes 240 nanoseconds. If the CPU requested data is not already in Cache, 4 bytes are fetched from Main memory and stored in Cache. The requested word is then passed directly to the CPU. Usually, the additional word fetched is the next instruction to be executed. This gives the CPU a look ahead capability which expedites task execution.

The Cache is divided into two groups, Group 0 and Group 1. Each group makes up 50% of the total Cache memory or about 1K byte. Disabling both groups of the Cache forces Main memory cycles for every fetch instruction. Disabling one group or the other reduces the effectiveness of the Cache. The effects of Cache memory on a 22K size task are shown below.

Cache Memory Status	Task Execution Time
Both groups enabled	7.58 seconds
Both groups disabled	17.95 seconds
Group 0 disabled	9.33 seconds
Group 1 disabled	9.11 seconds

It is obvious from the data that the Cache effectively shortens execution times.

2.2.1.4 Internal Data Paths

Internal data paths are designed for high performance having a 32-bit parallel data bus (Massbus) that can interface a mass storage device via a Massbus controller, and 16-bit data paths for interfacing medium to low performance peripherals.

The Massbus transfers 32-bits plus 4 parity bits (one per byte) in parallel between Main memory and Cache memory or 4 bytes of data between Main memory and a high performance peripheral such as a disk drive or a 9-track tape drive.

2.2.1.5 Memory Management

Memory Management (MM) provides the hardware facilities necessary for memory relocation and protection. Address modification is the main function of MM. The hardware converts 16-bit program generated virtual addresses to 22-bit physical addresses. MM receives all virtual addresses generated by the user program, relocates them if necessary, and then transmits the physical address to the Cache or Unibus. MM can access all physical address locations in Main memory.

In a multi-programming system, MM provides the means for assigning memory pages to a user's program and preventing that user from making unauthorized access of other assigned pages. Each individual page has a protection or access key associated with it that defines access to that page: read/write or non-read/write.

2.2.1.6 Unibus Map

The Unibus Map is the interface between the Unibus and Cache memory. It performs the address conversions that allows peripheral devices on the Unibus to communicate with physical memory. Responding as a slave device to Unibus signals, the Unibus Map converts the 18-bit Unibus address to a 22-bit Cache address. The TOAS computers can each address 512K words or 1.024 Mbytes through the use of 31 read/write registers 22-bits long.

2.2.1.7 Unibus

The Unibus is a 56 line bus that connects the processor, memory, all peripherals, and allows for communication and data transfer between system components. Addresses, data, and control signals are transmitted along the Unibus. The form of communication on the Unibus is the same for every supported peripheral. Communication between devices on the bus take a master-slave form.

During any Unibus operation, one device has control of the bus. The bus master is the controlling device communicating with a slave device. Every device on the Unibus capable of becoming the bus master possesses an assigned priority level. A device request arbitrator located in the Cache memory unit (independent of Cache) determines whether the Cache will perform a processor, Unibus Map, or a Main memory access. The Unibus arbitration is accomplished by regulating bus requests and transferring bus control to the requesting device which becomes the bus master. For simultaneous bus requests of equal priority, the requesting device electrically closest to the processor becomes the bus master after the current bus master releases the data section of the bus.

The maximum data transfer rate on the Unibus under optimum conditions is one 16-bit word every 400 nanoseconds, or 2.5 million 16-bit words/second.

2.2.2 Main Memory

The TOAS computer system memories consist of DEC MJ11-A magnetic core memory and add-on Intel IN-1670 semi-conductor memory. Each computer system memory, shown in Figure 2-5, consists of 64K words of MJ11-A and 448K words of IN-1670. The two memories are accessed via the Main Memory Bus.

Cache memory is the controlling bus master for Main memory. The Cache determines which word in memory will be accessed by placing the 22-bit address of the word on the Main Memory Bus address lines. Memory read or write operations are also determined by the Cache.

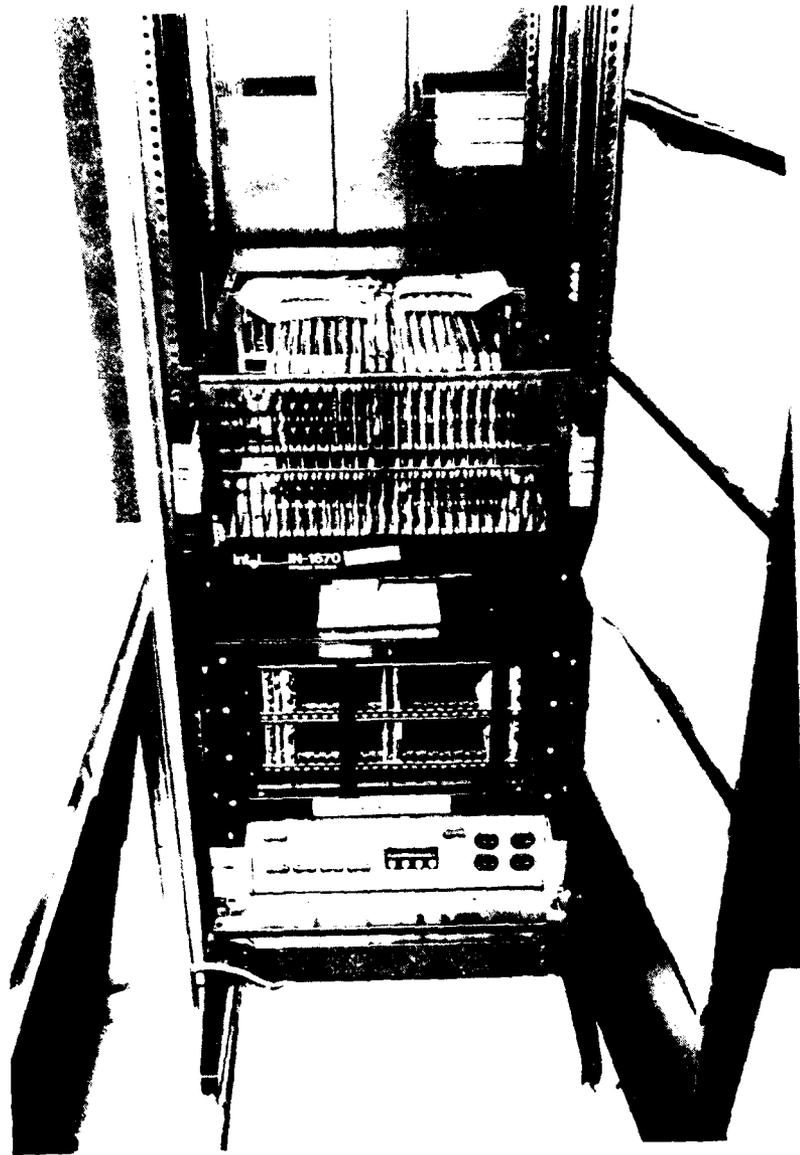


Figure 2-5. Main Memory - IN-1670 (top),
MJ-11-A (middle), Power Supply (bottom)

2.2.2.2 MJ11-A Magnetic Core Memory

The MJ11-A memory is a read/write random access memory based upon coincident current, non-volatile, magnetic core. Access time is typically 750 nanoseconds with a complete cycle time of 1080 nanoseconds. During a MJ11 cycle, 2 words (36-bits) of data are transferred in parallel to the Cache memory. The MJ11 controller consists of the M8148 Memory Control and Timing module and the M8149 Memory transceiver card.

Memory controller can be broken into two major functions: address recognition and control/timing generation. The controller examines the address that the Cache puts on the Main Memory Bus and determines if the address falls within the response range of the memory controller. If the address is within the response range, the module will initiate a memory cycle when it receives a MAIN START signal on the Main Memory Bus.

2.2.2.2 IN-1670 Intel MOS Semi-conductor Memory

The IN-1670, shown in Figure 2-6, is an add-on memory for the PDP-11/70. The memory device is composed of 16 MU-167 boards. Each MU-167 board contains 80 Intel 2108 dynamic 8K metal oxide silicon (MOS) random access memory (RAM), integrated circuit packages. Each MU-167 supplies 32K words of RAM. The TOAS Intel memory units each support 14 MU-167s yielding 448K words of additional memory. This memory combined with the 64K of MJ11 supports each computer system with 512K words of RAM.

The IN-1670 is expandable to 512K words in 64K increments or two MU-167 boards. A total of 2 Megawords could be added to the PDP-11/70 with each 512K words requiring 10.5 inches of mounting space in a standard DEC rack.

The memory unit features high performance, error coding, error correction (ECC), error monitoring, and single/double bit error logging. The memory cycle time is 790 nanoseconds for read and write allowing maximum throughput. Additional speed could be attained by interleaving memory giving a 20-30% effective increase in memory bus width. At present, the TOAS computers do not support interleaved memory.



Figure 2-6. Intel IN-1670 MOS Semiconductor
Memory (448K Words)

The error logging facility records the corrected single-bit errors by storing information about the location of the failing 8K RAM integrated circuit responsible for the error. Double-bit errors are also logged in the same manner, giving information as to the locations of the chips responsible. A double-bit error is recorded but not corrected. A double-bit error condition will force the CPU into an error state. The error logging board is located with the MU-167 boards.

Two additional boards are required for system operation. The control card receives interface signals and address inputs from the Cache memory. It generates the internal control signals required by the system and also checks the address parity in addition to normalizing the address inputs. The data board transfers read/write data between the Cache and the MU-167 boards. It generates write data check bits which are stored along with the write data, and checks read data parity correcting single-bit errors.

2.2.3 Controllers/Interfaces

Controllers and interfaces serve two important functions. Controllers direct large amounts of data to or from memory at the highest possible transfer rates. Data is transferred between high-speed peripherals such as a disk drive or magtape transport and memory via a high-speed controller. The PDP-11/70 supports accommodations for four RH-70 Massbus controllers or similar high performance controllers.

An interface serves as the communications link between the computer and other devices. Interfaces serve to translate signals sent from one device into signals that the receiving device can interpret. Most interfaces serve to electrically link I/O terminals to the computer.

2.2.3.1 RH-70 Massbus Controller

The RH-70 is an extremely fast and reliable Massbus I/O controller interfaced with Cache memory and the Unibus. Major functions of the RH-70 include: communications with Main memory via Cache in order to store and fetch large amounts of data; communications with the CPU via the Unibus to receive commands, provide error and status information, and to

generate interrupts; and interface with one to eight compatible mass storage disk drives via the Massbus. The RH-70/Cache interface routes 22 address bits, 36 data bits (2 words and 4 parity bits), and three control signals.

The controller is divided into two major functional groups: the Register Control Path (RCP), and the Data Transfer Path (DTP). The RCP allows the program to read/write any one of six registers contained in the RH-70 via the Unibus. The DTP consists of 8 word x 16-bit, first-in/first-out memory buffer and associated control logic. This memory buffers data in order to compensate for fluctuations in the cycle arbitration time of the Cache.

To transfer data, the CPU signals the particular controller via the Unibus and read/writes the RH-70 control registers. The RH-70 then issues a Request to Cache signal. The Cache boards also support the request arbitrating logic which selects one of the four RH-70s based on an assigned priority (controller A having the highest priority and controller D the lowest priority). If the requesting controller is selected for the next memory cycle, the Cache asserts the appropriate information onto the RH-70/Cache interface. In most cases, the RH-70 will transfer double words from memory.

2.2.3.2 BR-1566/BR-1569 Controller/Multiplexer

The BR-1566 is a high-speed Memory Bus interface similar to the RH-70 and occupies the RH-70 #C slots in computer system A. This device is used in conjunction with the BR-1569 Communications Control Unit (CCU). The CCU is a 32 channel I/O multiplexer designed to interface a variety of local serial and remote peripherals to the PDP-11/70 via the BR-1566. The BR-1566 can interface up to four BR-1569 CCUs.

The TOAS Facility supports a BR Controller/Multiplexer on computer system A. The BR-1569 supports the necessary hardware to realize eight active channels designated as BM channels. Additional hardware is necessary to support additional BM channels. The BM software channels are

numbered BM0: through BM31: while the actual hardware channels are numbered J1 through J32. The BM handler is the software routine that addresses the 32 I/O ports.

Available protocols on the 8 active channels are given below.

Channel	Protocol	Baud Rate
J1-BM:0	SU-CRC	9600
J2-BM:1	TTY ASCII ODD	9600
J3-BM:2	SU-CRC	9600
J4-BM:3	WU PTC AUTODIN	2400
J5-BM:4	SU-CRC	9600
J6-BM:5	TTY ASCII ODD	9600
J7-BM:6	SU-CRC	9600
J8-BM:7	WU PTC AUTODIN	2400

2.2.3.3 DL11-E Asynchronous Line Interface

The DL11-E is a character-buffered data communications interface designed to assemble or disassemble the serial bit stream required by a data terminal I/O device. Parallel character data can be disassembled sent serially to be reassembled at the receiving terminal and vice versa.

The unit consists of a single quad module that can be mounted in either a Small Peripheral Controller (SPC) slot or in one of the DD11-DK Peripheral Mounting Panel slots. The TOAS Facility (System B) supports 4 DL11-E interfaces shown in Figure 2-7. These interfaces support CRT terminals and graphic display terminals.

The DL11-E is the most versatile of the DL11 family. It uses call and acknowledge signals from the computer and data set, to establish a handshaking sequence and thus maintain a communications channel. The data format consists of a start bit, 5 to 8 data bits, 1 odd or even parity bit or no parity bit, and 1, 1.5, or 2 stop bits. The baud rate is variable from 200 to 9600 baud.

2.2.4 System Peripherals

Most computer system peripherals and components connect to and communicate with each other on the Unibus. The central processing unit uses the same set of signals to communicate with Main memory and system



Figure 2-7. DLL1-E Asynchronous Line Interfaces

peripherals. The system peripherals also use this same set of signals when communicating with the processor, memory, or other peripherals. Each system peripheral has an assigned address on the Unibus.

2.2.4.1 RP06 Disk Drive

The RP06 disk drive is a high speed, large capacity storage device designed to operate on-line with the PDP-11/70. Two RP06 drives are shown in the right of Figure 2-2. Features include: Bad Block Files to ensure data integrity; blocked data transfer which improves system throughput by reducing the number of data transfer requests; dual access options that allow rapid manual switching between controllers; Error Correction Code (ECC) that increases data reliability and improves throughput; and write checks to verify data integrity.

Two major parts comprise the functional RP06 drive: the disk storage drive and the Device Control Logic (DCL). The disk storage drive houses the circuits for: rotating the disk pack; positioning the 19 read/write heads (plus one servo read head) at the addressed cylinder track and sector; and writing/reading data on the disk pack surface. The disk pack has 19 recording surfaces that are divided into 815 cylinders per pack. Each cylinder is divided into 19 tracks. An unformatted disk pack can store 107,520 bits per track. A formatted pack has a 176 Mbyte storage capacity.

Prerecorded track information allows the servo read head to locate the 815 cylinder positions so that the read/write heads are able to transfer data to or from a particular track. The average seek time is 30 milliseconds with a nominal data transfer rate of 6,448,000 bits/second off of the 3600 rpm disk pack.

The DCL attaches to the side of the drive assembly and is composed of three main subassemblies: the interface logic card nest and Massbus cable connections; the power supply; and the power monitor. The card nest contains eight cards, six of which convey signals between the DCL

and Massbus A/Massbus B. The two remaining cards convey signals between the DCL and the disk drive and are referred to as the minimum device level interface (MDLI).

Dual access capabilities are controlled by the DCL which permits access by two different RH-70 controllers. When the drives are set in the dual access mode, it allows drive access by either controller on a first come, first serve basis. When the first come controller finishes accessing the drive, the DCL is released to place the drive back in a device available status.

The RH-70 Massbus controller is interfaced to the DCL via 22 16-bit registers with 6 registers in the RH-70 and 15 registers located in the DCL. There is one register shared between the RH-70 and DCL. A read/write to the registers is accomplished under program control via the Unibus.

2.2.4.2 TWE16/TME11-EA Magtape Transports

Magtape transports provide the TOAS Facility with mass, off-line data storage capabilities. The transports are shown in Figure 2-2. Magtape provides the means to economically enable the facility to back-up vital system information in the event that an operating system on disk was inadvertently wiped out.

The TWE16 is an industry-compatible 9 track magnetic tape transport system. The TWE16 comprises a master transport with interface and control logic, and a TE16-EA slave transport. The master transport interfaces with Main memory through a RH-70 Massbus controller. Also contained in the master transport is the TM03 formatter. The CPU communicates with the TM03 via the Unibus.

The TE16 is capable of reading and writing on tape at 1600 bits/inch in Phase Encoding (PE) mode and 800 bits/inch in NRZI mode. Tape density and character format are program selectable. Forward and reverse tape speeds are 45 inches/second and 150 inches/second respectively. Maximum data transfer rate is 72,000 bits/second.

The TME11-EA is a 9 track tape system (TMB11/TE10) that has been modified to a 7 track format. The TMB11 controller interfaces the Unibus to one TE10 tape drive. Each computer system supports one TME11-EA. The TE10 has a read/write capability of 800 bits/inch at a forward tape speed of 45 inches/second and a maximum data transfer rate of 36,000 bits/second. Rewind speed is 150 inches/second.

2.2.4.3 Pertec D3442 Disk Drive

The Pertec D3442 moving head disk drive shown in the left of Figure 2-8 is a front loading disk cartridge rotating magnetic media drive. The magnetic media is composed of a fixed platter and a removable



Figure 2-8. Pertec Disk Drive (left), Imlac PDS-4/L Terminal (middle), and XEROX 1750 (right)

platter cartridge. Platter surface read/write is accomplished by four moving heads utilizing the double frequency method of recording data. The double density recording method writes at 2200 bits/inch and 200 tracks/inch.

The D3442 is intended for use with a DMA controller on small to medium size computers. The TOAS Facility utilizes the D3442 as a mass memory peripheral for the Imlac PDS-4/L Graphics Display Terminal mini-computer (16-bit). The PDS-4/L interfaces the D3442 and direct memory access (DMA) controller through a 36 line 3M bus.

Data transfer rates are 1.56250 Mbits/second or 195.3 Kbytes/second. Average seek time for one-third head stroke (read/write head moves along the disk radius) is 40 milliseconds while adjacent track seeks take 10 milliseconds. A full stroke seek takes 65 milliseconds.

2.2.4.4 LP11-VA Line Printer

The LP11-VA shown in Figure 2-9 is a free standing line printer designed to operate with the PDP-11/70 and associated Unibus peripherals. The printer contains a paper advance mechanism, top-of-form control, self-test capability. Hard copy output is produced at 300 lines/minute from an impact mechanism and continuously rotating 132 column, 64 character drum. Paper and ink pass between a row of hammers (one solenoid actuated hammer per two columns) and the character drum.

The LP11 controller interfaces the line printer to the Unibus, and is under program control. The controller is a single quad module that occupies one of the four slots in the DD11-DF back plane. The controller does not store information but synchronizes the data transfer between the line printer and the Unibus. The main controller functions are: indicate to the PDP-11/70 the operational status of the LP11; control data transfer from the PDP-11/70 to the line printer; and enable the line printer to gain control of the Unibus so that it may perform an interrupt service routine.

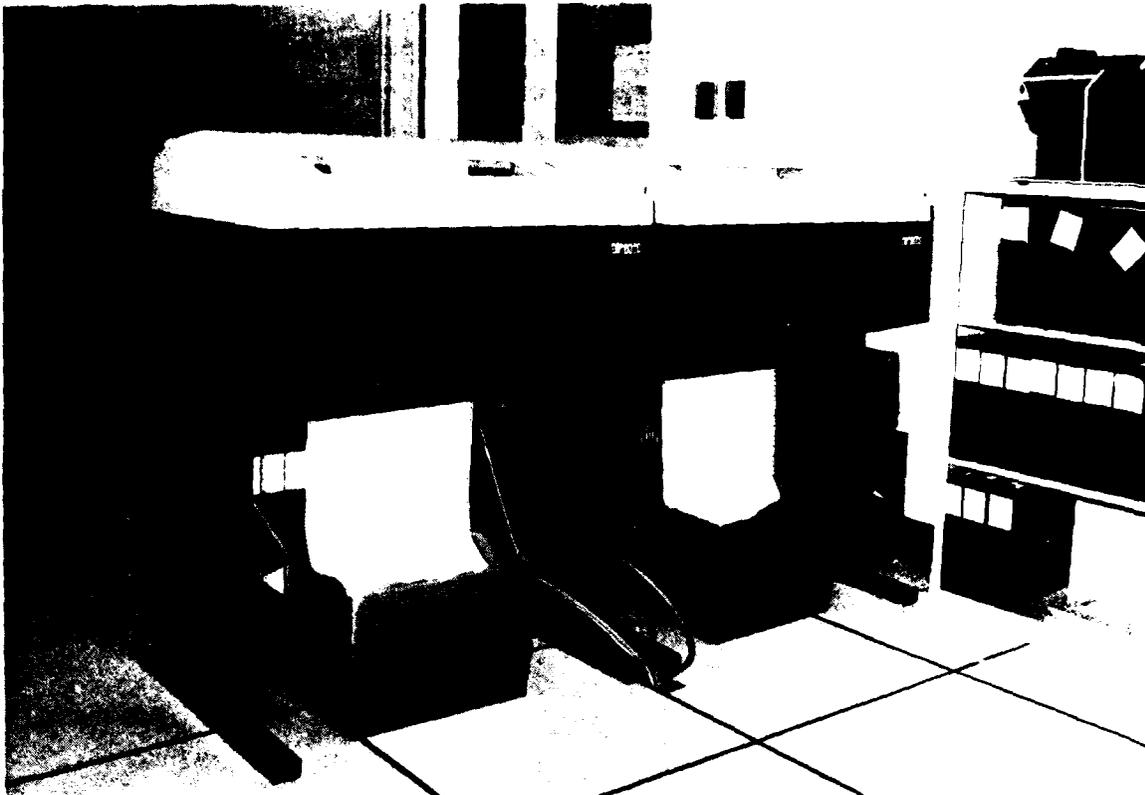


Figure 2-9. LP11-VA Line Printer

Two registers are located in the controller, one for printer status, and the other for the ASCII character to be printed. Data to be printed is 7-bit ASCII code transferred in parallel to a 144 x 8 bit data buffer one character at a time. After 132 characters have been loaded, the printer waits for a control character (which signals the line to be printed is complete) and ignores additional characters.

2.2.4.5 CR11 Card Reader

The CR11 shown in Figure 2-10 is a 285 card/minute, standard 12-row, 80 column card reader with a hopper capacity of 550 cards. The cards are sequentially separated from the stack and moved past a phototransistor

read station where the data is recognized in a serial, column by column manner. The cards are then stacked in the output hopper in the same order as input.



Figure 2-10. CR11 Card Readers

The reading cycle is under external program control for single cycle or continuous run. A single cycle is 200 milliseconds long, and will continuous run as long as the pick command remains active. A status register and two data buffers comprise the Unibus communication logic. The data buffers present the card data in two formats, compressed 8-bit and non-compressed 12-bit formats. The CR11 controller provides the command and monitoring functions for the reader in addition to handling data transfers

from the card reader to the Unibus. Two of the three registers are located in the controller. The controller occupies a small peripheral controller (SPC) slot in the BA11-FK mounting box.

2.2.4.6 PC11 Paper Tape Reader/Punch

The PC11 Reader/Punch and control comprises a PC05 high-speed reader/punch and a PC11 controller. The PC11 is capable of reading 8-hole tape at 300 characters/second and punching at 50 characters/second.

The reader is composed of: a light source; a photodiode read station to translate the presence or absence of punch holes into logic signals representing 1s and 0s; a tape transport mechanism to move and position the tape between the light source and read head; and bins to collect the tape passed through the reader. The punch comprises: a punch drive motor; a punching mechanism that translates logic levels into the presence or absence of punch holes; and a tape advancing mechanism to position the tape under the punch head.

Data is parallel transmitted from the reader to the controller (located in a SPC slot) when the reader reads, encodes, and transmits one byte of data from a frame on the paper tape. In the reader, the translated data is stored in a buffer that can be read by the computer. An output to punch operation is initiated when the processor transfers a byte in parallel to the punch buffer. When the punch mechanism is ready to cycle, the buffer is read and the character is punched.

2.2.5 User Terminals

The TOAS Facility supports three types of user terminals. The privileged LA36 system consoles allow direct manipulation of system functions and system configuration. The console terminal is for operator use and not general users. The PDS-4/L is a stand-alone terminal that can be down-line loaded and used as a timesharing Program Development System (PDS). The SU-1652M is a dedicated terminal supported by dedicated System A.

2.2.5.1 LA36 DECwriter

The Digital LA36 DECwriter is an interactive data communications terminal. Designed as an I/O terminal, the TOAS Facility uses the LA36 as a console terminal.

Hardware features include a low-speed impact printer for hardcopy output on variable width line printer paper, and a standard ASCII keyboard. The keyboard options include variable baud rates (110, 150, and 300 baud), cap locks, numeric keypad, and a line/local setting.

Output is 30 characters/second throughput via a 16 character buffer and a 60 character/second catch-up mode. The character generation hardware consists of a 1K byte character generator ROM, and a solenoid actuated impact printer head yielding a 7 x 7 dot matrix. The LA36 is connected to the processor by a DL11-E asynchronous serial interface.

2.2.5.2 SU-1652M Dual Screen Monitor

The 1652 (Figure 2-11) is a 15 inch dual screen micro-programmable terminal used to manually prepare, display, edit, and enter data/control signals to the PDP-11/70 via the BR1569 Communications Control Unit. In addition, the 1652 supports alphanumeric and/or graphic displays sent from the PDP-11/70.

The terminal is provided with a light pen, dual VFK (60 keys), and interactive graphics options (joy stick). The Intel 8080 microprocessor provides terminal intelligence. Down-line loading of complete programs is attained via the Program Load Module (PLM).

2.2.5.3 Imlac PDS-4/L Graphics Display Terminal

The PDS-4/L in conjunction with the Pertec D3442 disk drive is a stand-alone, refreshed-graphics, interactive display as shown in Figure 2-8. Features include: a Display processor that is programmed in its own assembly language for generating displays; a Main processor for file I/O, field calculations, and other support functions.



Figure 2-11. SU-1652 M Dual Screen Terminals

Hardware features include: a 67 key programmable alphanumeric keyboard, rapid refresh display (40/second), a random deflection 21-inch CRT, and complementary software. The Pertec disk drive supplies 10 Mbytes of mass rapid access memory. In addition, the PDS-4/L can output text to an on-line Xerox 1750 printer.

2.3 SOFTWARE TECHNICAL DESCRIPTION

The baseline system software consists of commercial DEC operating systems and compilers, the GRAPHELP graphics system (Harry Diamond Laboratories), and Imlac Utilities. The baseline system software modules consist of:

- Interactive Applications System (IAS) (DEC)
- Data Base Management System (DBMS-11) (DEC)
- DECnet-11 (DEC)
- COBOL-11 (DEC)
- FORTRAN IV PLUS (DEC)
- GRAPHELP
- IMLAC MODULES
- UNIVAC MICRO CODE

These software modules are available for use by Project 2315 participants when working at the TOAS Facility. Due to copyright restrictions, the above software cannot be provided for use outside of the TOAS Facility. The following sections provide a brief description of the baseline system software capabilities.

2.3.1 Interactive Application System (IAS)

IAS is DEC's general purpose operating system implemented on the PDP-11/70 processor. It is a multi-user timesharing system that supports concurrent interactive, real time, and batch applications. The TOAS Facility has IAS Version 3.0 operating in the timesharing mode; the other operating system modes (Real-time and Multi-user) could be generated if required.

IAS can provide timesharing services for up to 32 simultaneous users and supports a variety of peripheral devices. The timesharing user/system interface is the Program Development System (PDS) which requests and processes passwords and user names to validate the users identity.

PDS allows the user to create, edit, and execute user programs and data files. In addition, PDS allows interaction with some system peripherals and utilities.

The interactive applications facility is easily modified and additional applications can be added. As a generalized, flexible base for executing interactive applications, IAS provides support for application specific user/system interfaces where it is necessary to present a custom interface to terminal users. The special purpose interfaces can be written and checked using PDS and then installed in the system for use on specific terminals.

Tabulated below are the system features supported by the different operating modes.

	Real-time	Multi-user	Timesharing
Priority Scheduler	X	X	X
Heuristic Scheduler		X	X
General Purpose Timesharing			X
Volume Protection			X
Program and Data Protection			X
User Written CMD Language Interpreter			X
Concurrent Real-time, Multiuser Program Development		X	X
Program Development System (PDS) With System Control Interface (SCI)		X	X
Monitor Console Routine (MCR)	X	X	X
Print Spooling	X	X	X
Reentrant Code	X	X	X
Sharable Data Areas	X	X	X
Utilities	X	X	X
Multitasking	X	X	X

IAS was built from RSX-11D operating system with Version 3.0 enhancements in terms of flexibility and functionality over the predecessors IAS Version 2.0 and RSX-11D. The significant major features are:

- Enhancement to the IAS/R SX-11D Executive. The ability to include the IAS heuristic timesharing scheduler into the Executive is supported.
- Addition of subtasking support at the Kernel Executive level via the SPAWN system directive.
- Support for the full complement of memory management directives (including dynamic creation, attach, and deletion of regions and inter-task transmission of region access).
- A more powerful user interface which supports both the DEC Command Language (DCL) and Monitor Console Routine (MCR) languages.
- A new, easier system generation procedure which utilizes a question and answer dialogue for selection of major options. For TOAS, the system generation magtape will not work unless the TME11 (7 track magtape system) controller is removed.

2.3.1.1 Executive Enhancements

The IAS/R SX-11D Executive has an integrated, IAS heuristic time-sharing scheduler. The heuristic scheduler allocates resources to inter-active tasks using a time slicing algorithm and dynamically computed priorities. The scheduler option will run tasks based on their past history of performance and degree of interaction. If necessary, the scheduler swaps tasks in and out of memory from an allocated swapping area on the system disk. The system manager has the ability to dynamically create and delete checkpoint swap files. The R SX-11D timeslicer was replaced by the heuristic scheduler.

The system null-task has been rewritten to run in the Kernel mode rather than the user mode. This eliminates context switching in and out of the null task.

Should a task node allocation failure occur, the Executive supports the ability to put a task into a wait-for-nodes state. This situation may arise either because the task would exceed its pool limit or because the system node pool is depleted. This feature is selectable as part of the system generation procedure.

2.3.1.2 Task Spawning

A task can invoke execution of other tasks with the option of receiving information regarding their termination status via the SPAWN directive. Tasks which are spawned may use the "exit with status" facility that writes information concerning the task status at exit time into an exit status block. Also, the issuing task can specify that an Asynchronous System Trap be queued or an event flag set to inform it that the spawned subtask has exited. The degenerate case of the SPAWN directive is the REQUEST directive.

There is no limit to the number of subtasks that a parent task may spawn. Spawned tasks may also spawn tasks. It should be noted that the task spawning facility is separate from that made possible on a full time-sharing system with the Timesharing Control Primitives (TCP).

2.3.1.3 Memory Management Directives

Using the Memory Management directives, user tasks may dynamically create sharable memory areas (regions) of any size. The regions may be checkpointed or swapped with a task. Regions may remain resident until explicitly deleted. The region size is limited by the amount of available physical memory.

A task may dynamically map regions (either entirely or a portion) as well as sharable global areas into a task's virtual address space at run time. Tasks may share the contents of a region with other tasks. Access to a given region may be "sent" from one task to another enhancing inter-task communications. Each region has associated protection, set up by its creator, which is the same format as the file protection used for disk files.

The directive support facility allows tasks of greater than 32K words to be entirely memory resident and dynamically mapped, thus reducing the number of disk accesses for overlaid tasks and enhancing performance. The directive supports FORTRAN-IV Version 2.0 virtual arrays up to 32767 elements.

2.3.1.4 User/System Interfaces

IAS supports the DCL (PDS) and MCR command syntax with almost every MCR command having a PDS analog. Real-time systems usually implement MCR as the user/system interface while multi-user systems utilize MCR or PDX. PDX is a special version of PDS; MCR is usually preferable to PDX due to space requirements for PDX. MCR has been changed to take advantage of the task spawning feature along with additional commands that have been added to enable users to access the new system features. The MCR indirect file processor allows the creation and use of interactive command files.

Full timesharing systems implement PDS and a MCR "mode". A PDS user terminal supports the MCR mode which was included for those users more familiar with MCR commands than PDS commands. However, the MCR mode does not have all the capabilities of a true MCR user/system interface.

The MCR interface is present on the system console after the computer is bootstrapped. Timesharing is then set in operation by executing an indirect IAS command file that installs the timesharing facility. The system console is automatically renamed the SCITERMINAL and the SCI interface prompt is presented to the user. SCI commands are privileged operator commands used to manipulate/control the operating system. The SCI task runs at priority 220 (priority 250 being the highest) which allows the operator to intervene in lower priority user tasks when necessary. For example, the operator can abort a looped program via the SCITERMINAL. SCI recognizes the full set of PDS commands and also supports the MCR mode interface.

2.3.1.5 System Generation

System generation procedures for IAS Version 3 are easier than previous versions of IAS/RXS-11D. A question and answer dialogue prompts the user for inclusion of major options. The terminal handler building procedures and device configuration procedures have also been simplified. An indirect command file is provided for the building sequence. These features allow the TOAS Facility operating system environment to be quickly changed to accommodate user requirements.

2.3.2 Data Base Management System (DBMS)

The DBMS is an implementation of the COBASYL data base language specification. The DBMS provides data control and manipulation functions for application programs. The application programs can be written in COBOL, FORTRAN, or other languages using the CALL statement.

DBMS supports network and hierarchical type data structures and permits structure definition suitable to the applications. It also provides a separate language facility, Data Description Language (DDL), for description of the complete data base or portion of the data base. For a detailed discussion of the DBMS concept, refer to the Data Base Administrator's Guide.

2.3.3 DECnet-11

DECnet is a software package that extends the IAS operating system to form computer networks. The DECnet facilities provide for program sharing and intertask communication. Peripheral devices from a remote system may be connected to a host computer system and used via DECnet. The files from the remote system may be shared or new files opened for storage.

An executable program module may be transferred to a remote system for execution (down-line loading or specific tasks). Intertask communication is allowed between two tasks, either locally or remotely.

2.3.4 COBOL Compiler

The COBOL compiler translates ANS-74 COBOL source into relocatable object modules. The compiler runs under the supervision of the IAS operating system and conforms to all connections and restrictions of IAS. To run a COBOL program, a five step process is required: 1. Prepare the source program. 2. Compile the source program. 3. Merge or prepare an overlay description file (optional). 4. Task-build the object modules into an executable task. 5. Execute the task. For a detailed description of COBOL use, refer to the COBOL User's Guide.

2.3.5 FORTRAN Compiler

The FORTRAN-IV Plus compiler is supported at the TOAS; however, FORTRAN-IV with virtual data arrays can be installed if required. For a detailed description of compiler use, compiler diagnostic messages, and the run time diagnostic messages, refer to the FORTRAN-IV Plus User's Guide. For a more detailed description of specialized applications, an Object Time System Reference Manual is provided by the Facility.

2.3.6 GRAPHELP

GRAPHELP is an interactive graphics FORTRAN-IV software package that runs on a PDP-11 computer system. The GRAPHELP package supports all Tektronix 401X Graphic Storage Tube Terminals and the Imlac PDS-4/L Refresh Graphics Display System. The software provides both absolute and relative vectors of four varying line textures, user definable scaling, windowing, clipping, terminal transparency, and 128 nested subpicture display files for refresh graphics. Routines are provided for interactive graphics crosshair input and screen erase control. The applications are oriented towards data plotting for both linear and logarithmic data, along with alphabetic and numeric symbol output. The documentation for GRAPHELP is obtained by printing all files with TXT extension located in UIC 210,1 . The GRAPHELP libraries referred to in the documentation (PLTFTN, TKGFTN, IMGFTN, ALLFTN) are built and located in UIC 1,1 .

2.3.7 Imlac Software

The Imlac PDS-4/L terminal system provides the user with powerful utility programs, editor, disk operation system, assembler, compiler, interface systems, emulator, and diagnostics that are used in the stand-alone mode. These software packages were delivered as part of the PDS-4/L system.

2.3.7.1 Disk Operating System (DOS-4)

The DOS-4 provides a monitor for control of the system programs and utility programs. The system allows for file maintenance and usage on the disk system as well as generation and execution of system and application programs.

2.3.7.2 System Editor (DFED)

The DFED is a powerful disk-scrolling (page) editor that can be used to edit programs and text. The editor supports individually specified Macros along with hardware defined context-editing commands. The editor can be used as a document-processing system when used with the Xerox 1750 printer.

2.3.7.3 Program Assembler (Compiler) and Linker

Typically, an ASCII version of a program is written using the disk fast-scrolling editor (DFED); then, the newly created source program is run through the Assembler (ASM) to produce either an executable object program or a block of relocatable code subsequently to be bound into an object program by the Linking Editor (BIND). A library of relocatable coded segments or modules can be created through use of the Relocatable Library Editor (LIBRED). If, during link editing, unresolved externals are discovered, the binder searches this library and inserts the referenced modules in the proper locations.

2.3.7.4 Editor Graphics (ED80)

The ED80 is an edit program with timesharing, graphics, and form control capability. The editor allows 80 characters per line with 40 to 80 lines on the screen. The editor runs in two modes of operation. Editor mode allows for alphanumeric and graphic text editing; form mode allows for protected areas of text on the screen.

2.3.7.5 Compiler

The Imlac system supports a FORTRAN-IV compiler. The compiler conforms to the ANSI X3.9-1966 specification except for the features listed below.

1. END Lines with spaces between the E, N, and D
2. COMPLEX numbers
3. STOPn
4. PAUSE
5. Adjustable array dimensions

6. External statement or function names as dummy arguments
7. DATA statements with arrays or repeated constraints
8. G format
9. BLOCK DATA Subprogram
10. Unlimited use of blank characters

Refer to the FORTRAN-IV Language Manual User's Guide for a description of how these features are affected.

2.3.7.6 Terminal Interface System (TIS)

The TIS was developed to use in conjunction with the United States Military Academy Graphics Capability System (GCS). A terminal interface is provided for user log on and communication with a host computer system with GCS.

The GCS has been obtained and examined for use with TOAS. The GCS is designed to run on a large host computer (CDC 6000, Univac 1108, Honeywell 635, DEC 10, and IBM 370) The GCS will not run on the PDP-11 without modifications.

2.3.7.7 Tektronix Emulator

The STR14 utility program emulates the Tektronix 4014 terminal. The enhanced graphic module features are supported for point-plot mode, special point-plot mode and incremental plot mode. The emulator can be used with the GRAPHELP library to run graphics routines and systems on the PDS-4/L terminal.

2.3.8 Univac Micro-code

The SU 1652 micro-code, supplied by the Univac Corporation, has been converted to Files 11 format and stored on the TOAS time sharing disk at UIC 210,11 . The micro-code for the terminal maintenance has been modified to allow it to be assembled on the PDP-11; an executable task module is located at UIC 210,1 .

In addition to the maintenance micro-code, the Program Load Module (PLM) contains a number of different micro-code packages that can be down loaded using the PLM routines. Refer to Section 5 for more information on the PLM utility.

3. FACILITY MANAGEMENT PROCEDURES

The purpose of this section is to provide the standards and guidelines for TOAS facility operation. This section is applicable to all contractor and government personnel using the TOAS facility and is effective upon publication and distribution. This document does not supersede any existing documentation but is intended as a guideline for orderly, efficient management of the TOAS facility resources. Other applicable documents include:

- TAC-RADC Memorandum of Agreement
- ESD-TAC Host Tenant
- Project 2315 Contracts
- ASPR Series Documents

3.1 PROJECT 2315

Project 2315 is an advanced Research and Development (R&D) effort sponsored by the Rome Air Development Center (RADC/IRDE). The program is designed to develop prototype equipment, techniques, and procedures to enhance USAF tactical operational intelligence functions and supporting processes. The program will also provide functional specifications, designs, alternatives, and prototype elements for follow-on systems. The TOAS Facility will be the focal point for conducting demonstrations of operational intelligence functions such as collection management, targeting, etc., along with validation of concepts and functional specifications.

3.2 FACILITY OPERATIONS AND PROCEDURES

The TOAS facility is the focal point of the Project 2315 Tactical Intelligence development and other RADC sanctioned R&D efforts. Since the facility is located within an Air Force tactical operations environment, developer-user interaction is promoted, and an increase in the timeliness and appropriateness of the R&D programs engineered and managed by RADC is expected. (See Figure 3-1 for project management structure).

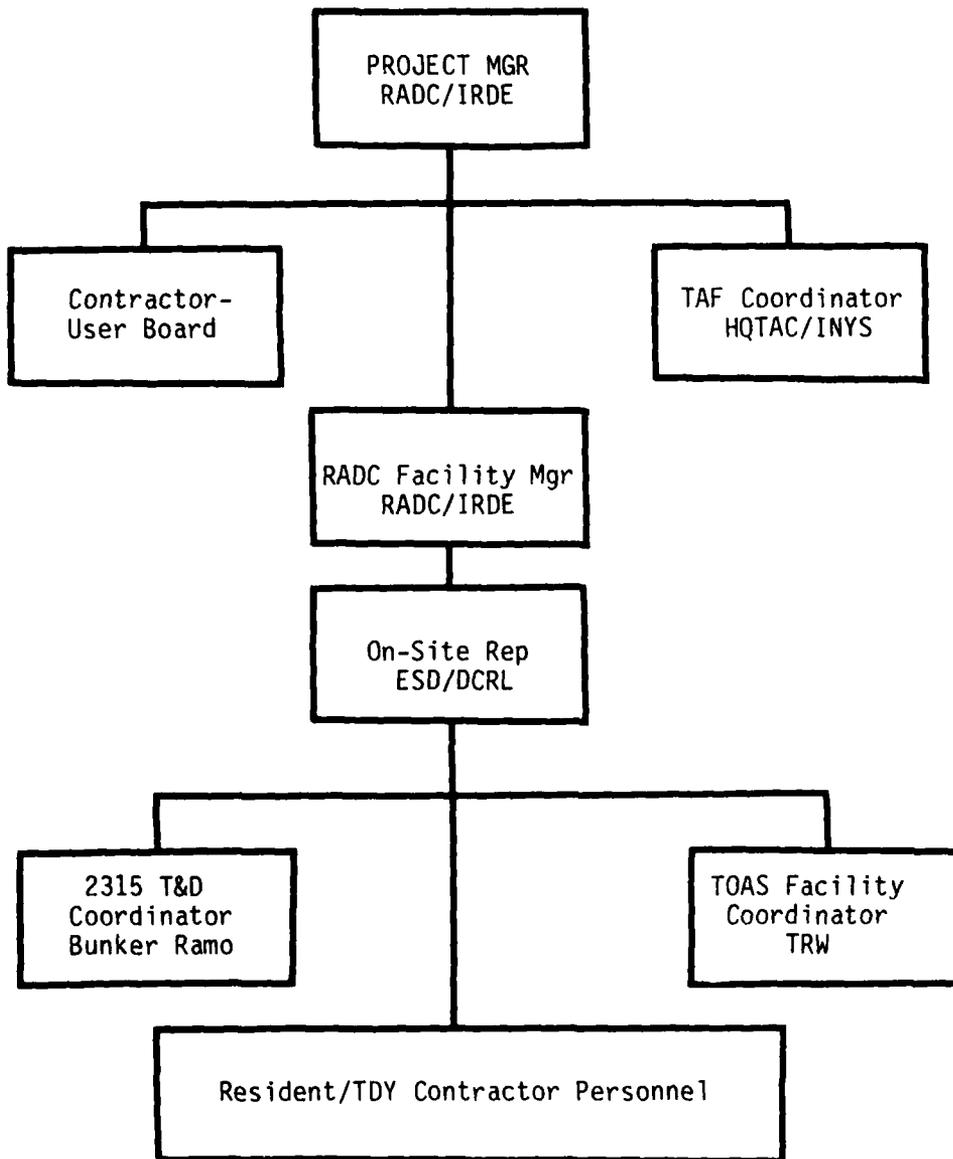


Figure 3-1. Project 2315 Management Structure

The facility, dedicated to R&D activities, will provide the flexibility to change software and hardware components with minimal constraints. The daily TOAS Facility operation is the responsibility of the Facility Coordinator, while overall operation is the responsibility of RADC. A list of project-related definitions is in Appendix 3-A to this section.

3.2.1 Hours of Operation

The facility will normally be open from 0700-1700 hours five days/week. The computer resources will be available to the users 0800-1600 hours 5 days/week. However, scheduling requirements for use of the computer resources beyond 8 hours/day shall be submitted to RADC/IRDE no more than 20 or less than 7 days in advance. Arrangements will be made to operate the computer resources for up to a maximum of 12 hours/day based on demand.

3.2.2 Security and Visitor Control

3.2.2.1 Physical Security

The TOAS facility is located in building 23 (Langley AFB, Virginia) which is approved for open storage of DOD Secret material. Unescorted entry into this building requires a Secret security clearance be filed with the 460 Reconnaissance Technical Squadron (RTS) Security Office which controls access to this building.

3.2.2.2 Visitor Control

All visit requests for purposes other than working with permanent resident contractors must be sent to:

HQ ESD/DCRL
BLDG 106
LANGLEY AFB, VA 23665

ATTN: MR K. H. SHINGLER

Unescorted entry into Building 23 can not be granted unless a valid security clearance (SECRET) is on file. If required, pass

sensitive compartmented information (SCI) clearances via appropriate channels to:

AFSSO TAC
PASS TO 460 RTS (ATTN: TOAS FACILITY)
LANGLEY AIR FORCE BASE, VIRGINIA 23665

3.2.2.3 Computer Security

Computer facility security will be the responsibility of the Facility Coordinator who will:

- Control access to computer resources
- Control classified output in accordance with established requirements
- Copy, store, and control software systems associated with facility operations
- Ensure good security practices are followed in the operation of the computer facility

Note: Due to limited space within the facility, permanent storage of classified documents by non-resident contractors is not possible.

3.2.3 Physical Facility Structure

The facility is divided into an office area and the computer area (see Figure 3-2).

3.2.4 Computer Hardware Operations

In order to provide the maximum flexibility and benefit to TOAS Facility users, the concept of open and controlled computer system will be implemented.

3.2.4.1 Open Computer System

An "open" computer system will be one that is dedicated to a single system user or dedicated to several users working together to demonstrate a single TACC task, e.g., collection management, targeting, etc. The TOAS Facility will be configured with dual PDP-11/70 processors. This may be a single system user for each CPU, or a single user may have control of both CPUs. During this period

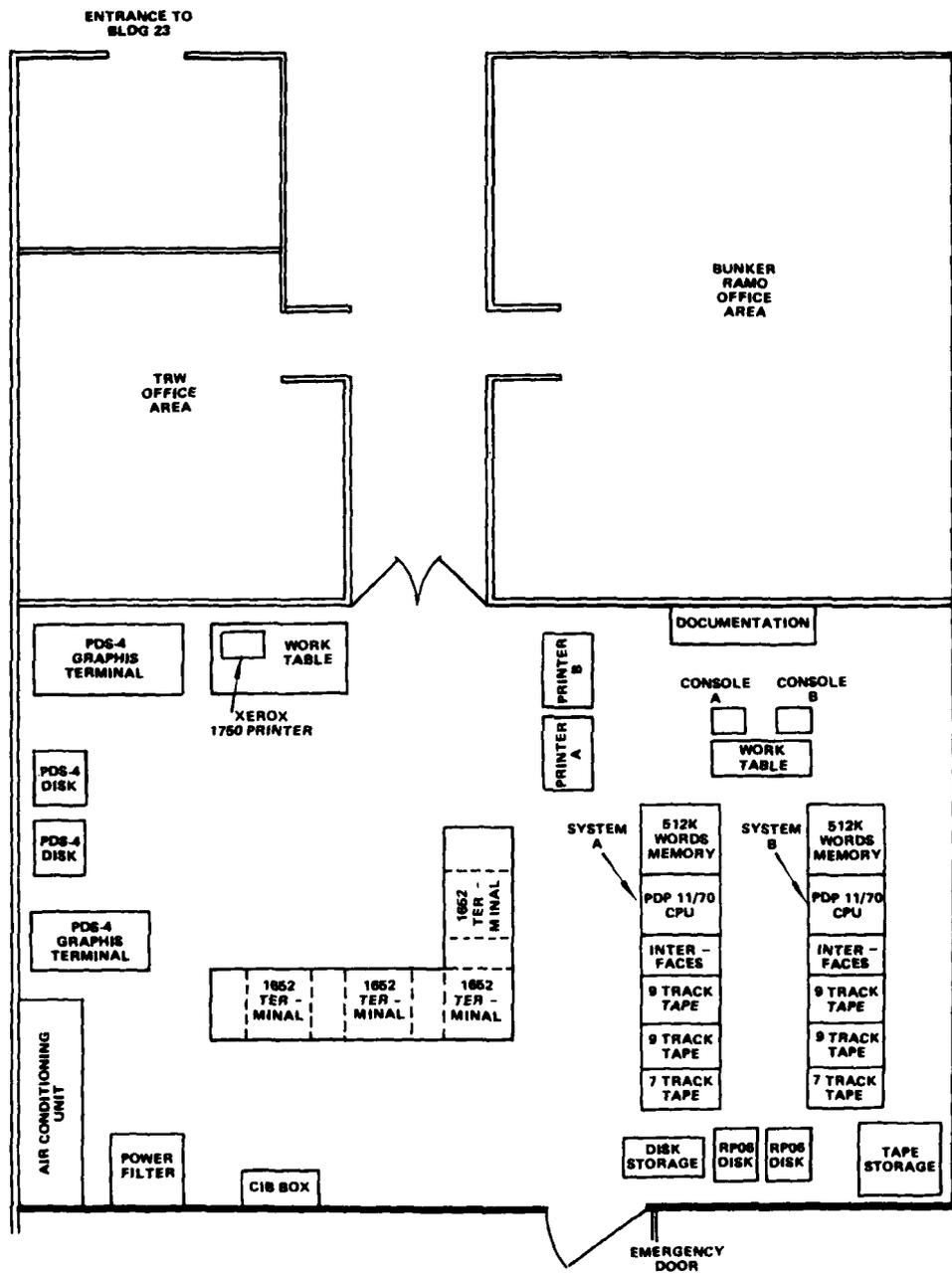


Figure 3-2. TOAS Facility Layout

the single user has direct access to all system component and peripheral devices (i.e. tape/disk drives, I/O devices, etc.). Computer operator services will be provided on an as requested basis only.

3.2.4.2 Controlled (Closed) Computer System

This system is configured to support several users in a time sharing environment. User services are provided by a computer operator assigned by the Facility Coordinator. Users will have access to tape and disk drives and system I/O devices. Support for program/file development is a typical application of this type of system configuration. It is anticipated that the "time share" environment will be periodically scheduled for daily usage.

3.2.4.3 Baseline System

The initial Project 2315 baseline will consist of the commercial hardware and software configuration items. As new software modules are developed, tested, and demonstrated, these modules may be added to the baseline with the Configuration Control Board (CCB) approval. The Facility Coordinator will store and maintain the baseline system and documentation as it is received from the developing agency. Interoperability of new software modules with the existing baseline will rest with the developing agency. The Facility Coordinator will also ensure that the baseline documentation is current and available at the facility.

3.2.5 Controlled Computer System Operation

Access to the computer area will be restricted to personnel working with the ADP resources. In order to efficiently utilize the ADP resources available to Facility users, the following administrative procedures will be followed.

3.2.5.1 Logs

A user log will be provided for each computer system (open system). System software will log users time on the closed system. Classified output will be logged by the computer operator.

3.2.5.2 User Identification Codes

Each facility user will be assigned a unique UIC and password by the Facility Coordinator. Passwords will be changed periodically.

3.2.5.3 Output

Printed output will be obtained from the TRW computer operator. Classified output will be handled in accordance with required security practices.

3.2.5.4 Expendables

The Facility Coordinator will insure that an adequate supply of expendable computer items such as paper, ribbons, etc are available within the facility.

3.2.5.5 Facility Cleaning

All individuals are responsible for ensuring their areas are kept clean and orderly. In order to maintain a high state of cleanliness there will be no smoking, drinking or eating in the computer area.

3.2.5.6 Scheduling

The Facility Coordinator will be responsible for publishing Weekly and Quarterly computer use schedules.

3.2.5.6.1 Quarterly Schedule

The Quarterly schedule will be prognosticated for a one year period and will include major events such as project demonstrations, experiments, and long term system development activities. Inputs to this schedule should be transmitted to RADC, who will determine requirements, hardware/software/manning/need for additional information/new or modified baseline applications programs, etc.; and performs/accomplishes contractor direction. RADC will then furnish the schedule to the on-site RADC Representative, who then makes up the weekly assignment of the TOAS assets and manpower in conjunction with the TOAS Facility Coordinator, T & D Coordinator, TAF Coordinator, and concerned contractors. RADC will coordinate and approve the weekly schedule.

The TOAS Facility Coordinator then publishes and distributes the quarterly schedule. This should be accomplished no later than four weeks prior to the beginning of the affected quarter. Failure to meet this deadline may have serious impact on computer use time available to the contractor project manager. This schedule will be coordinated and approved by RADC prior to distribution.

3.2.5.6.2 Weekly Schedule

The purpose of the weekly schedule is to efficiently manage computer hardware and software assets in satisfying Quarterly schedule data and the inputs received the week prior to the affected timeblock. "Fact of life" changes will occur on a daily basis - both good and bad which will affect the schedule. All schedule conflicts will be adjudicated by the RADC Facility Manager.

3.2.5.6.3 Site Documentation

A library of documentation will be established for all users of the facility. This documentation will include reports/studies of participating contractors, facility handbooks, user software manuals, etc. It is the intent to have available on-site documentation to support the development activities. An index will be provided and suggestions for items for inclusion are solicited subject to security considerations.

3.3 TECHNICAL/FUNCTIONAL DEMONSTRATIONS

The procedures for conducting a test/demonstration for government personnel will follow the above procedures with the modifications listed in this paragraph.

3.3.1 Sponsor

Each technical/functional demonstration will have a primary contractor sponsor who will have overall responsibility for defining the demonstration. The sponsor will be required to coordinate with the T&D coordinator for contractor/government participation, test plans, scheduling system availability (and configuration), and conducting the demonstration.

3.3.2 Test Plan

The test plan must be coordinated by the players and approved by RADC.

3.3.3 Test/Demonstration Output

The test plan will specify disposition of magnetic media and hardcopy output generated during the test period. Classified materials will be controlled in accordance with local security practices.

3.4. CONFIGURATION MANAGEMENT

In order to design and develop software modules that interoperate efficiently and accurately, close coordination will be required among the contractors producing software for demonstration/test. The formal management procedure for insuring interoperability will be the Configuration Control Board. The site CCB is a sub-board of the RADC CCB.

3.4.1 Configuration Control Board

The Configuration Control Board (CCB) will consist of contractor representatives developing software for demonstration on the TOAS facility hardware and a government representative who will act as the Chairman. Others may participate at the discretion of the Chairman. Meetings will be held as required at the TOAS facility and/or in conjunction with the Project 2315 Quarterly Review meetings.

3.4.2 Terms of Reference

The objectives of the Project 2315 CCB is to insure that new software development is compatible with current baseline software for demonstration; approve new software for the baseline; and provide a forum for technical contractor coordination; and to ensure software specifications proposed for demonstration are consistent with Project objectives/milestones. The intent of the CCB is to approve changes to the baseline after successful demonstration and present acceptable alternatives to RADC. Detailed procedures for CCB operation are provided in Appendix 3-B of this section.

3.5. TRAINING.

Project 2315 training is the responsibility of the Test and Demonstration Coordinator and will be provided to all essential government and contractor personnel involved with the demonstration/testing of Project 2315 baseline applications package software. The specific nature of such training is discussed in the Project 2315 Training Plan. All other training is the responsibility of the individual agency or contractor.

3.6. MAINTENANCE.

3.6.1 Hardware

The TOAS Facility Coordinator is responsible for preventive and corrective maintenance. A hardware Maintenance Log will be maintained by the Facility Coordinator to provide a record of hardware problems. When users encounter a suspected hardware malfunction, they must document the problem in the Maintenance Log. Four hours of preventive maintenance is scheduled each week.

3.6.2 Software

The initial baseline software system provided to the TOAS facility will be maintained by the Facility Coordinator. As new software releases are provided by Digital Equipment Corporation, the baseline software modules and associated documentation will be updated. A review of the new modules by the CCB will be required prior to incorporation as the 2315 baseline software. Other baseline software modules and associated documentation will be updated/changed by the developing/sponsoring contractor upon approval of the CCB. Interoperability issues will be resolved through the CCB forum. Maintenance of the baseline facility software library does not encompass corrective maintenance of individual software modules provided by other vendors. Operating problems which indicate the need for software repair or modification will be documented as specified in the Configuration Control Plan and forwarded to the appropriate module developer for appropriate action.

APPENDIX 3-A: PROJECT 2315 DEFINITIONS

3-A.1 BASELINE SYSTEM

Defines the software and hardware that RADC designates as required to support the development, evaluation, and demonstration of Tactical Air Force functions, e.g., collection management, targeting, etc., and/or communications and external/internal displays. Once established, the hardware and software components of the baseline system will be controlled by RADC through the use of the configuration control function.

3-A.2 CONFIGURATION CONTROL BOARD

The CCB is composed of Project 2315 contractor and government representatives. The purpose of this board is to control the hardware and software configuration available for RADC approved tests and demonstrations. This board will operate as a subcommittee of the Project 2315 Contractor Coordination Group.

3.4.3 RADC FACILITY MANAGER

RADC (or its designated representative) is the Facility Manager and has the overall and final authority over Project 2315 matters. The Facility Manager is responsible for providing equipment, property, and services required by on-site contractors; ensuring appropriate long range coordination is effected between contractors; providing required funding for facility equipment, operations, and services. The facility manager coordinates and approves long-term facility scheduling requirements and adjudicates scheduling problems.

3-A.4 TOAS FACILITY COORDINATOR

TRW has been designated as the Facility Coordinator. The Facility Coordinator prepares and maintains the facility operating schedule. Coordinates on test and demonstration plans to ensure the required baseline hardware and software is available and appropriately configured.

Provides computer operations and maintenance activities as outlined in paragraph 3.2. Establishes and manages the facility baseline configuration in accordance with the Configuration Management Plan (Appendix 3-B). Provides copies of the baseline software to other agencies when approved by RADC.

3-A.5 ON-SITE RADC REPRESENTATIVE

A permanent Air Force Systems Command employee authorized by RADC to represent them in Project 2315 matters, at Langley AFB. Responsible for coordinating the facility utilization schedule (including test and demonstration); functions as the liaison between contractor and Langley Air Force Base personnel. Monitors contractor on-site performance. Further responsibilities of this representative are contained in the latest TAC Headquarters and RADC memorandum of agreement.

3-A.6 TACTICAL AIR FORCES COORDINATOR

TAC/INY is responsible for coordinating tactical Air Force (TAF) user (TAC/PACAF/USAFE) inputs and participation for Project 2315 demonstrations/experiments.

3-A.7 RESIDENT CONTRACTOR PERSONNEL

Those personnel permanently assigned to the TOAS facility. TRW and Bunker Ramo provide resident contractor personnel.

3-A.8 TEST AND DEMONSTRATION COORDINATOR

The Bunker Ramo representative has been designated by RADC as the Test and Demonstration (T&D) Coordinator for Project 2315 applications software.

3-A.9 TDY CONTRACTOR PERSONNEL

Those persons working on Project 2315 contracts requiring periodic use of the TOAS Facility and its computer resources.

APPENDIX 3-B: CONFIGURATION MANAGEMENT PLAN

3-B.1 OBJECTIVE

The objective of this plan is to establish formal procedures for the effective management and control of the Project 2315 baseline software and hardware.

3-B.2 SCOPE

This plan applies to users of the RADC Tactical Operations Analysis Support (TOAS) facility involved in Project 2315 demonstrations/experiments.

3-B.3 RESPONSIBILITIES

3-B.3.1 Rome Air Development Center (RADC)

The RADC Project Manager (RADC/IRDE) is responsible for insuring contractor compliance with the terms and provisions of this plan. The on-site Langley AFB RADC/ESD representatives will provide Government-Contractor liaison and assistance on all matters concerning policy interpretation.

3-B.3.2 Project 2315 Contractors

All contractors charged with Project 2315 experiment/demonstration responsibilities or participation must comply with the terms and intent of this plan in the performance of their respective tasks.

3-B.3.3 Configuration Control Board (CCB)

The CCB is a separate sub-board of the Project 2315 Contractor Coordination Board and is charged with the administration and execution of this plan.

3-B.4 CONFIGURATION MANAGEMENT ORGANIZATION

Responsibility for the configuration management of Project 2315 baseline hardware and software rests with the Project Manager who is also the CCB chairman. Final Approval authority, however, will remain with the Project 2315 Project Office (RADC/IRDE) and their Facility Manager.

3-B.4.1 Configuration Control Committee (CCC) Membership

The CCC is composed of the following representatives:

- An RADC/IRDE representative, or designee, who will be the Chairman
- The resident RADC/ESD representative, who will be the Vice Chairman
- The TOAS Facility Coordinator (TOAS Facility Contractor)
- The 2315 Applications Test and Demonstration Coordinator (Applications Contractor)
- Other 2315 Contractors, as required, by invitation of the Chairman
- Recording secretary appointed by the Chairman.

3-B.4.2 CCB Membership Responsibilities

Each member of the CCB is empowered with a single vote for the purpose of conducting the business of the committee. A majority vote will be considered binding on all committee members. Voting will normally be restricted to CCB policy matters and will not be applied to technical matters under consideration by the committee. The specific duties and responsibilities of CCB members are described in the following paragraphs. Any decisions which impact or potentially impact on contractual obligations will be forwarded to the RADC Project Office for review and processing.

3-B.4.2.1 Chairman

The Chairman of the Configuration Control Board is responsible and has operational authority for the conduct of the committee. All instructions and operating procedures concerning configuration management policy emanate from his office. He will be responsible for:

- Developing and implementing working level procedures which define the methods used to control the computer software developed for the TOAS Facility
- Providing assistance in design reviews and interpretation on all matters concerning configuration management
- Reviewing proposed facility software/hardware change requests, Engineering Change Proposals (ECPs) and Specification Change Notices (SCNs) after submission to his office
- Ensuring product releases are in conformity with facility operations requirements
- Reviewing all data deliverables for conformity with facility library requirements
- Having the CCB review all proposed changes
- Maintaining all configuration management program related data
- Resolving all conflicts which arise at the CCB
- Establishing the date, time and place of the CCB meetings and insuring that adequate meeting facilities are provided
- Referring items which arise during CCB meetings, but are beyond CCB control, to the appropriate project element or other agency for review or action
- Recommending modifications to the TOAS Facility hardware configuration
- With TOAS Facility Coordinator concurrence, approving modifications to the TOAS software baseline (Software Library).

3-B.4.2.2 Vice Chairman

The CCB Chairman or Vice Chairman will convene and conduct all meetings of the Configuration Control Board. He will be responsible

for insuring that all items tabled before the CCB are fully discussed and properly disposed of. Unless otherwise designated, the Vice Chairman will assume the duties of the CCB Chairman in his absence.

3-B.4.2.3 General Membership

The general membership of the CCB will consist of the Project 2315 hardware and software contractor representatives required to properly evaluate the technical matters under consideration by the committee. Not all contractors will be represented at every CCB meeting. Contractor representation is mandatory when items tabled before the committee are within their area of responsibility. The designated representative will be empowered with the decision-making authority of the contractor represented. The general members of the CCB will be responsible for reviewing all agenda items.

3-B.4.2.4 Recording Secretary

The CCB Recording Secretary will attend all official meetings of the committee. The Recording Secretary will be responsible for:

- Recording and publishing the minutes of all CCB meetings
- Collecting and processing all items to be included on the CCB agenda
- Preparing and delivering to all CCB members, a list of all agenda items to be discussed at the next scheduled meeting
- Maintaining a status report of all CCB assigned action items and their suspense date

3-B.4.3 CCB Tasks

The Configuration Control Board will be tasked with the following duties:

- Reviewing all recommended enhancements, as well as program and documentation error reports included on the agenda, to determine the validity thereof

- By majority agreement, recommend approval, disapproval, refer or defer for future action each item on the agenda
- Assign and schedule each approved modification for installation
- Review software/hardware test results/reports and provide recommendations concerning the change

3-B.4.4 CCB Method of Operation

The CCB will be convened as required, to review baseline configuration changes. Meeting will normally be scheduled in conjunction with the quarterly contractors review meeting. These meetings will be presided over by the Chairman or a designated representative.

Each new suggested system enhancement, program problem report, or document error report will be screened by the CCB to insure that the following requirements have been met:

- Each report is accurately presented, and the originator's intent is understood
- A documented report is not a duplication of a previous recommendation or request
- Specific references/documentation requirements are complete and correct
- All reports constitute a valid recommendation or request and are technically sufficient to warrant an evaluation or analysis.

Following the determination that the above requirements have been satisfied, the CCB will assign a change number (CN) to the approved change. Those reports and recommendations not deferred for suspended action by the CCB, or outside CCB purview, will be scheduled for implementation at a later time. Reports/recommendations requiring system redesign action will be scheduled for implementation as soon as practical following estimated design completion. Reports referred to other parties for review will be scheduled for reassessment pending outside reply.

The CCB will periodically review the status of all open reports and recommendations that have been assigned for members resolution. In this manner, real and/or potential problem areas may be identified, discussed, and properly resolved.

Periodic CCB meetings will be convened specifically to review the software change schedule for the purpose of insuring that changes have been correctly scheduled in accordance with their importance. Should the CCB determine that any report or recommendation submitted for its evaluation does not fulfill the requirements previously outlined in section 4.4, the committee will recommend a disposition or corrective action and route the request back to the originator accordingly. Such action may include, but is not limited to:

- Rejecting the request as being technically undesirable or infeasible
- Requiring further clarification or expansion
- Scheduling the request for consideration at a later date
- Determining the request as outside CCB authority and forwarding to the appropriate party or agency.

When, as a group, the CCB can not decide on any question or problem within the purview of the group, the impasse will be resolved by the Chairman as the final authority on configuration management issues.

3-B.5 BASELINE HARDWARE/SOFTWARE CONFIGURATION

3-B.5.1 Baseline Software

The master copy of the Baseline software will reside at the TOAS Facility and controlled by the TOAS Facility Coordinator. This baseline will not be an integrated system, but will consist of various files and/or modules. Release of a copy of the baseline software (or subset) will be under direction of RADC or the on-site RADC representative, subject to contractual and security controls.

3-B.5.2 Baseline Hardware

The hardware configuration will be controlled by the TOAS Facility Coordinator who is responsible for computer maintenance. Upon request, the hardware configuration will be documented to insure consistent system performance during experiments and tests.

3-B.5.3 Delivery/Installation of Baseline Changes

As changes are approved by the CCB, the tasked contractor will be responsible for providing a fully integrated software product on magnetic tape. As systems evolve, the master baseline software products or modules will be provided to the TOAS Facility Coordinator as replacement vice change tapes.

4. FACILITY MAINTENANCE PROCEDURES

This section describes the preventive and remedial maintenance procedures applied to the TOAS Facility. The procedures are performed on the computer system hardware according to a maintenance plan/schedule that is unique to each electronic component or module. The plan consists of scheduled preventive maintenance inspections including the performance of system software diagnostics.

Sections 4.1 through 4.3 provide an overview of preventive maintenance inspection (PMI) tasks, diagnostic software components, and troubleshooting procedures. Subsequent sections detail activities for the individual components.

4.1 PREVENTIVE MAINTENANCE INSPECTION

The TOAS Facility maintenance philosophy is structured to provide a minimum of eight hours/day of computer service to TOAS Facility users. This goal is achieved by maintaining the facility equipment in a clean and highly reliable state by accomplishing periodic PMI on computer equipments.

PMI provides the TOAS Field Engineer with information on the overall system condition and potential problems in individual system components. This information can be used to investigate possible problem areas and initiate repairs before operating schedules are disrupted.

The required frequency and type of PMI is directly related to the type of equipment, environment, and usage. As the amount of on-time increases, PMI requirements must also be accomplished on a more frequent schedule.

Preventive Maintenance Inspections are accomplished at the TOAS Facility in accordance with the equipment manufacturer's suggested PMI schedule and the Facility's published operating schedule.

4.2 DIAGNOSTICS

Diagnostics are programs executed by the PDP 11/70 processor to monitor and report the hardware reliability of the system component. Diagnostics monitor the 11/70 CPU, memory, busses, controllers, and peripherals such as disk units, line printers, card readers, paper tape reader/punch, magtape transports, and I/O terminals.

The value of periodic diagnostic sessions is the ability to diagnose problem areas and prevent potentially fatal errors from occurring within the system.

The TOAS Facility supports three major types of diagnostic packages: MAINDEC-11, MPG, and IAS/RXS-11D. Each package has unique applications on different system components. However, overlap does exist. The overlap can be put to an advantage by comparing diagnostic results from two different packages run on the same target device.

4.2.1 MAINDEC-11 (CZQXALO XXDP Users Manual)

XXDP is a "catch-all" name for a group of PDP-11 diagnostic software packages available on the TOAS diagnostic disk pack. The XXDP diagnostics can be run individually or run as a chain of individually executed programs.

Also included in the MAINDEC-11 diagnostic package is DEC/X-11. DEC/X-11 is a system exerciser that can be configured to any PDP-11 system. System interaction exerciser programs drive associated systems at maximum activity rates in order to provoke noise, timing, and logical interaction failures. The advantage of this type of exerciser is that the system is operating in a normal, but highly active way. This will force malfunctions to become apparent that might not be when a stand-alone diagnostic is run.

4.2.2 Maintenance Program Generator

The maintenance program generator (MPG) diagnostic tool allows the user to write diagnostic programs that suit a particular task. MPG can support simultaneous execution of up to sixteen user programs. This

capability (much like DEC/X-11) is useful in troubleshooting interaction problems or for allowing concurrent troubleshooting of individual device problems. The user is required to specify the task and/or data operations that are to be performed by his program.

MPG is available on the MAINDEC-11 XXDP diagnostic package.

4.2.3 IAS/RSX-11D Diagnostics

The TOAS Facility operates and maintains an Interactive Applications System (IAS) operating system environment. IAS provides two complementary methods of monitoring the hardware reliability of the system. The first method, error logging, allows error statistics to be compiled for main and cache memory, disks, and magnetic tape. Printed reports are available detailing or summarizing hardware errors on the above devices. The error logging is continuous; printed reports are obtained when desired.

The second method of monitoring hardware reliability is to run software diagnostic tasks to test specific devices. These tasks execute simultaneously with other system functions and user tasks. Therefore, the timesharing system can continue to service computer users as PMI is accomplished. If the resident software error logger indicates that a device is malfunctioning, device specific diagnostic tasks should be accomplished.

Two types of diagnostics are included in the system: diagnostic programs and data reliability tests. Each device for which diagnostics are available has an associated diagnostic program and a data reliability test.

The data reliability tests perform a subset of the functions in the diagnostic programs. They do not provide the capability to select the subtests to be performed as can be done in the diagnostic programs. Additionally, they do not allow selection of conversation mode. Conversation mode permits dynamic interaction with the diagnostic test.

The diagnostic programs and data reliability tests must be task built (linked) before they can be installed and run. Task building is

required to allow specification of variables such as the specific unit to be tested and the buffer size to be used. To facilitate the building process, an interactive program (called CMD) is provided. Diagnostics may be built, the task images stored, then used when needed. Special handlers in conjunction with the diagnostics pass error information to the diagnostics for interpretation and printing of error messages.

4.3 TROUBLESHOOTING

Troubleshooting is the process of isolating equipment malfunction to the smallest possible subsystem. This subsystem may be a printed circuit card or an individual component. Troubleshooting is usually incorporated with diagnostic results and maintenance manual direction.

The TOAS Facility supports the basic equipment to initiate troubleshooting procedures: digital volt meter (DVM), oscilloscope, diagnostic aids, and maintenance manuals. Troubleshooting is a complex procedure that requires equipment operation familiarity in order for it to be a time effective solution.

Because the TOAS Facility contains two identical systems, the board swapping technique is often the fastest method of malfunction isolation. After the suspected boards have been exchanged, diagnostic aids can be used to verify the same malfunction is occurring in the other hardware equipment. Corrective action can then be taken to repair or replace the defective component.

4.4 MAJOR SYSTEM COMPONENTS

When preventive maintenance is performed on a major system component the result is entered into a maintenance log. The log is a permanent record of all maintenance activities. Maintenance activities cover the following major system components:

- PDP 11/70 CPU/Memory
- Disk Drives
- Magtape Transports

- Card Readers
- Paper Tape Reader/Punch
- I/O Terminal

4.4.1 CPU/Memory

The KB11-C CPU is a 32 bit, 16 general register unit with options such as cache memory, memory management, double precision floating point processor and high performance peripheral controllers. The memory is composed of 128K bytes of DEC Core Memory and 896K bytes of Intel MOS memory.

4.4.1.1 Preventive Maintenance Inspection

Preventive maintenance procedures consist of running a sequence of diagnostic aids. See section 4.4.1.2 .

4.4.1.2 Diagnostic Descriptions

The PDP 11/70 CPU and memory are tested in succession. The CPU is thoroughly tested before proceeding on to the memory.

The CPU diagnostics test the bootstrap, floating point processor, and contain various exercisers. The memory tests are two point: The cache memory tests and the Intel memory test. The Intel memory also has an on-line error logging capability which records single and multiple bit errors. The specific diagnostics are listed below:

CPU

- DEKBH-A-D (EKBH) DIAGNOSTIC/BOOTSTRAP (M9301-YC)
Pattern: The program tests the basic CPU instructions. It will set the stackpointer, check and turn on memory management, the Unibus Map, and check memory from virtual address 1000 to 157776. After the memory is verified with the cache memory off, the cache memory is enabled and tested. If the test on cache fails, pressing continue will cause forced misses in both groups of the cache memory before going on to the bootstrap section of the program.

- DEFPA-A-D (EFPA) FP11C FPP Part 1 - DEFPA-B-D (EFPB) FP11C Part 2: These programs are designed to detect and report logic faults in the FP11-C Floating Point Processor (FPP). The tests are designed and sequenced to detect and attempt to identify logic faults at a minimum hardware/software level.
- DEKBA-B-D (EKBA) CPU Diagnostic Part 1 - DEKBB-C-D (EKBB) CPU Diagnostic Part 2: EKBA/B detect and report logic faults in the CPU through two stand-alone tests.
- CEQKCCO (EQKC) CPU Instruction Exerciser: This program makes a comprehensive check of the CPU cluster. The program executes each instruction in all address modes and includes tests for traps, interrupts, the mapping box, memory management, memory, the Unibus, and the Massbus.

MEMORY

- DEKBC-B-D (EKBC) Cache Memory Diagnostic Part 1: This program is used for the repair and maintenance of the cache memory system. This test checks of the four cache boards: Cache Control Board (CCB) and Cache Data Paths (CDP) board. Part 2 of this diagnostic should be run immediately.
- DEKBD-C-D (EKBD) Cache Memory Diagnostic Part 2: This program checks the remaining two of the four cache boards: Cache Address Memory (ADM) board and cache Data Memory (DTM) board. Part 1 of this diagnostic should be run first to obtain reliable results from this diagnostic.
- DEKBE-B-D (EKBE) Memory Management Diagnostic: This program tests the memory management logic and helps to isolate problems down to a replaceable module. The CPU and cache have been tested and are assumed error free.
- DEKBF-B-D (EKBF) Unibus Map Diagnostic: This program assumes that the CPU, cache, and memory management diagnostics have been run. The program will detect all errors that originate with the map box and provide loop capabilities for module isolation.

- DEMJA-C-D (EMJA) PDP 11/70 Memory Test: This program tests contiguous memory address from 000000 to 17757776. It verifies that each address is unique and that each location can be read/written reliably. It is also used for adjust/margin memory, and assumes DEKBA through DEKBF have been run.

4.4.1.3 Troubleshooting Procedures

Troubleshooting consists of isolating the malfunction to a replaceable printed circuit board by proper diagnostic aid interpretation.

4.4.2 RP06 Moving-Head Disk Drive

The RP06 Moving-Head Disk Drive is a large capacity, high performance, direct access disk file that uses an IBM 3336-11 removable disk pack with a 176 million byte storage capacity. The nominal data transfer rate is 806K bytes/second with an average seek time of 28 milliseconds.

4.4.2.1 Preventive Maintenance Inspection

PMI on the RP06 consists mainly of inspecting (refer to Figure 4-1) and cleaning. A maintenance flow chart is shown in the DEC disk drive technical manual. The inspection/clean outline is shown below.

1. Heads
2. Pack access door tracks
3. Door stops for wear
4. Shroud and spindle area
5. Air filter
6. Door lock for pin/rail clearance
7. Logic and power supply fans
8. Wind tunnel position
9. Lamp test
10. Air baffle
11. DC voltages at back panel

4.4.2.2 Diagnostic Descriptions

The following MAINDEC-11 diagnostics should be run for a complete inspection of the RP06 and the RH70 controller. They are listed in the recommended order of execution:

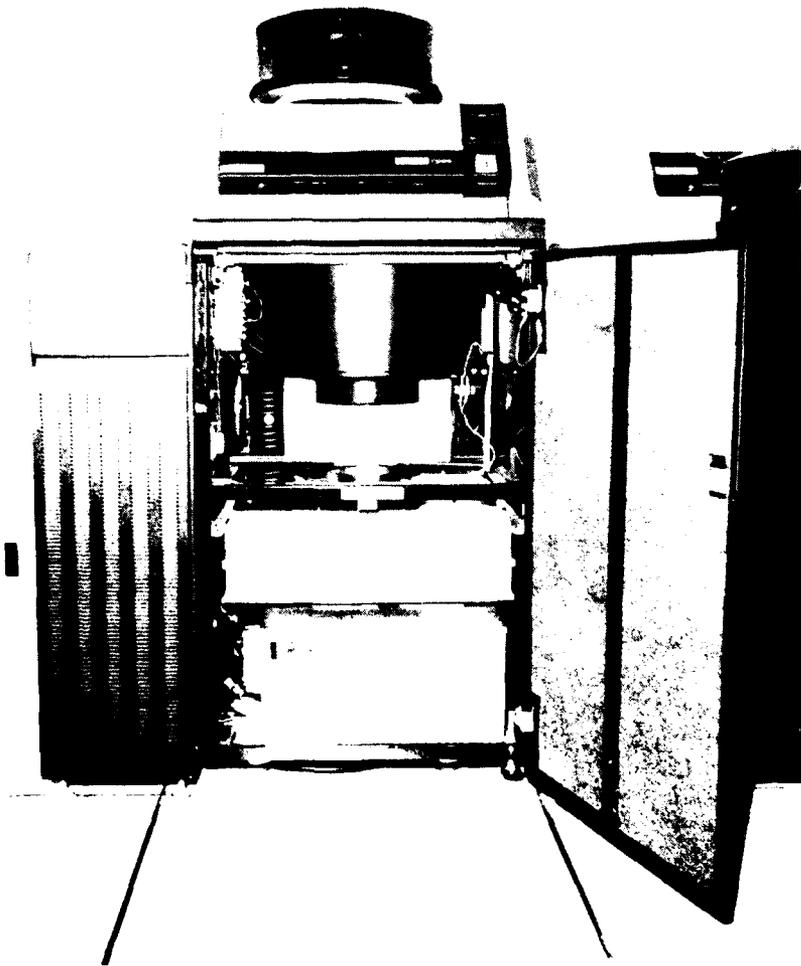


Figure 4-1. RP06 Disk Drive

- ERHADO (ERHA) RH70 - Controller Test:
This program verifies that the RH70 controller is operating correctly.
- ZRJGCO (ZRJG); ZRJHCO (ZRJH) - Diskless Controller Tests (Parts 1 and 2): This program tests the RH70 and Device Control Logic (DCL) portion of the RPO6. The DCL is used to make the RPO6 Massbus compatible and must be plugged into the Mass Device Level Interface (MDLI). The MDLI is the interface that connects the DCL to the disk drive assembly.
- ZRJICO (ZRJI); ZRJICO (ZRJJ) - Functional Controller Test: This program tests the DCL portion of the RPO6. It exercises the disk surface and mechanics of the drive to prove proper operation of the subsystem. A scratch disk pack must be used, which does not need formatting. DZRJG, DZRJH, and this test successfully run in this order prove the DCL circuitry works while not connected to the rest of the subsystem.
- DZRJE (ZRJE); DZRJF (ZRJF) - Dual-Port Logic Test (Parts 1 and 2): These programs check the dual-port logic in the DCL portion of the drive and require a special adaptor cable.
- ZRJCBO (ZRJC) - Head Alignment Verification: This program checks the RPO6 head alignment. An error is a misalignment greater than specifications.
- ZRJACO (ZRJA) - Mechanical Read/Write Test: There are 15 tests. Tests 0-6 check seek operations; 7-12 measure rotational speed, one-cylinder seek, average and maximum seek times; 13-14 check sector and track address circuitry; 15 checks data storage and retrieval capability.
- ZRJDCO (ZRJD) - Multi-drive Exerciser: This disk drive exerciser works up to eight RPO6 disk drives attached to the same RH 70. All data transfer commands are used. At the completion of each operation the program checks the RH 70. Formatted disks are required.

4.4.2.3 Troubleshooting

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The RP06 disk drive troubleshooting can be performed with the aid of the fault isolation charts in the technical manual and in conjunction with the diagnostic results.

4.4.3 Pertec D3000 Disk Drive

The D3000 disk drive is used in conjunction with the Imlac PDS-4 graphics display terminal. The disk drive contains two platters, one fixed (volume 0) and the other removable (volume 1). The removable disk is a cartridge type. Total storage capacity is 10 million bytes at 5 million bytes per platter. An average seek time is 40 milliseconds with a data transfer rate of 200K bytes/second.

4.4.3.1 Preventive Maintenance Inspection

A visual inspection of the disk drive for loose electrical connections, dirt, cracks, binding, excessive wear, and loose hardware should be conducted. The inspection list is given below:

1. Heads and disks
2. Pre-filter
3. Lubricate static discharge
4. Drive belt
5. Air filter
6. Lubricate catch assembly ball studs in bezel
7. Spindle magnetic chuck and cone
8. Positioner
9. Circumferential and radial alignment
10. Base casting

Steps one through seven should be performed at twice the frequency that steps eight through ten are performed. Refer to the maintenance manual for alignment procedures.

4.4.3.2 Diagnostic Descriptions

Diagnostics are available on the removable disk cartridge. The applicable diagnostics are shown below. Pertec manufactures a disk cartridge that is used for circumferential and radial alignment.

- TDISK - Test for Bad or Weak Disk Sectors: TDISK tests the two disk volumes for bad or weak sectors.
- RDISK - Disk Hardware Test: This test checks disk hardware by doing a single read-write per sector with the number of read-write attempts specified by the user. An error message is given when a bad sector is found. The message gives the sector location and nature of the error.
- RDVOL - Disk Hardware Test: RDVOL is subset of RDISK, the only difference being that RDVOL makes up to 16 read-write attempts per sector.
- CHECK - Sector Occupied Table (SOTB) Check: The CHECK program allows inspection of the disk-handling-software reliability.
- DIDL - Disk Octal Debugger: This diagnostic can be used to investigate the reason for a program blow-up. DIDL allows for the examination of the Imlac PDS-4 core memory and peripheral memory (Pertec disk drive). Memory tracing to a certain address is allowed at which time the address contents may be examined. In the examine mode, core or disk memory can be examined or modified. This diagnostic is useful in deciding if the disk is read/writing properly.

4.4.3.3 Troubleshooting

Fault isolation can be accomplished with the Pertec disk drive manual which supplies extensive troubleshooting charts. The charts list problem, possible cause, and recommended repair.

4.4.4 TE16/TE10 Magtape Transports

The TE16 is a 9 track, 45 ips, 800/1600 bpi tape unit and the TE10 is a 7 track, 45 ips, 800 bpi tape unit.

4.4.4.1 Preventive Maintenance Inspection

The DEC Magtape Transport preventive maintenance consists of inspection and cleaning of the head and tape path. The inspect/



Figure 4-2. 12/16/88 Magnetometer Analyzer

clean list (refer to Figure 4-2) is given below:

1. Tape transport mechanism
2. Read/write head
3. Erase head
4. Tape cleaner
5. Roller/guides
6. Vacuum pockets
7. Rubber capstan wheel
8. Hubs
9. Vacuum pump brushes

4.4.4.2 Diagnostic Descriptions

The MAINDEC-11 diagnostic - DNRZI (NRZI) - TE16/TE10W/TE10 - will run on any DEC Magtape system. The test should run for 10 minutes. If any soft errors occur, the operator is notified via the MCR console.

4.4.4.3 Troubleshooting

Troubleshooting the DEC Magtape Transport is accomplished by referring to the maintenance manual and the diagnostic results.

4.4.5 PC11 Paper- Tape Reader/Punch

The PC11 High Speed Reader/Punch, shown in Figure 4-3, reads an 8-hole perforated paper tape at 300 characters/second while punching tape at 50 characters/second.

4.4.5.1 Preventive Maintenance Inspection

The preventive maintenance on the PC11 is extensive due to the amount of moving mechanical parts. Procedures consist of inspecting moving parts for wear or breaks. All parts removed or replaced during inspection must be lubricated with the specified lubricant and installed in their original location. A clean brush should be used to remove dirt, paper dust, chafe, and other foreign matter from the unit.

Outlined below are the major areas of inspection:

1. Tape deflector plate
2. Platen
3. Tape guide
4. Idler pulley assembly
5. Tape guide support.



Figure 1. Control panel for the 40 inch

Disassembly and reassembly procedures are outlined in the manufacture's technical manual.

4.4.5.2 Diagnostic Descriptions

The DECX/11 diagnostics below should be used to exercise the reader/punch.

- CXPABFO (XPAB) - PA611 Punch Module: PAB exercises up to 16 high speed punches by punching a standard binary count pattern on each punch.
- CXPAAF0 (XPAA) - PA611 Reader Module: PAA exercises up to 16 high speed paper tape readers by reading a standard binary count pattern.

4.4.5.3 Troubleshooting

Troubleshooting can be accomplished by using diagnostic results in conjunction with the reader/punch maintenance manual. The adjustment procedures are outlined in the technical manual to maintain the PC11 in proper mechanical condition.

4.4.6 CR11 Card Reader

The CR11 is a standard 12-row 80-column card reader. The input hopper holds 550 cards of 7 mil thickness and reads 285 cards/minute in continuous run.

4.4.6.1 Preventive Maintenance Inspection

The PMI of the CR11 card reader consists primarily of routine cleaning. A cloth or paper wipe should be used to remove glaze and ink buildup. Below is shown the areas which require cleaning.

1. Picker sector - clean vacuum holes
2. Casting assemblies - clean card track
3. Cooling fan - clean intake screen
4. Exterior cleaning - soap and water only
5. Lubrication - rotary solenoid rollers

Consult the card reader technical manual for adjustment procedures.

4.4.6.2 Diagnostics Descriptions

The diagnostic - DZCRA-B-D (ZCRA) - should be used to exercise the CR11. This test is to be used as a card reader diagnostic. It tests all logic functions and includes an exerciser for all alphanumeric and binary test decks.

4.4.6.3 Troubleshooting

Troubleshooting the M-200 card reader can be accomplished by the use of troubleshooting charts listed in the card reader technical manual. The charts list symptom, cause, and remedy. The charts should be used in conjunction with diagnostic results.

4.4.7 LP11-VA (LP05) Line Printer

The LP11, shown in Figure 4-4, is a 64 character, 132 column width, 300 line/minute line printer.

4.4.7.1 Preventive Maintenance

Preventive maintenance on the LP11/LP05 is important because of the amount of moving mechanical parts. Below is the PMI list in the suggested order of execution.

1. General cleanliness
2. AC input voltage is within 10%
3. Cooling blower is operational
4. Verify DC voltages under load conditions
5. Test alarm indicator circuits
6. Ribbon drive system
7. Hammer bank position system
8. Paper feed system
9. Drive belt tension
10. Correct data and printing quality

For more detailed information consult the maintenance manual.

4.4.7.2 Diagnostic Descriptions

Diagnostics procedures on the LP11/LP05 use the internal self-test capability and the software diagnostic, DZLPK-H-D (ZLPK). This test checks out the processor interface control logic and the inter-communications data paths.

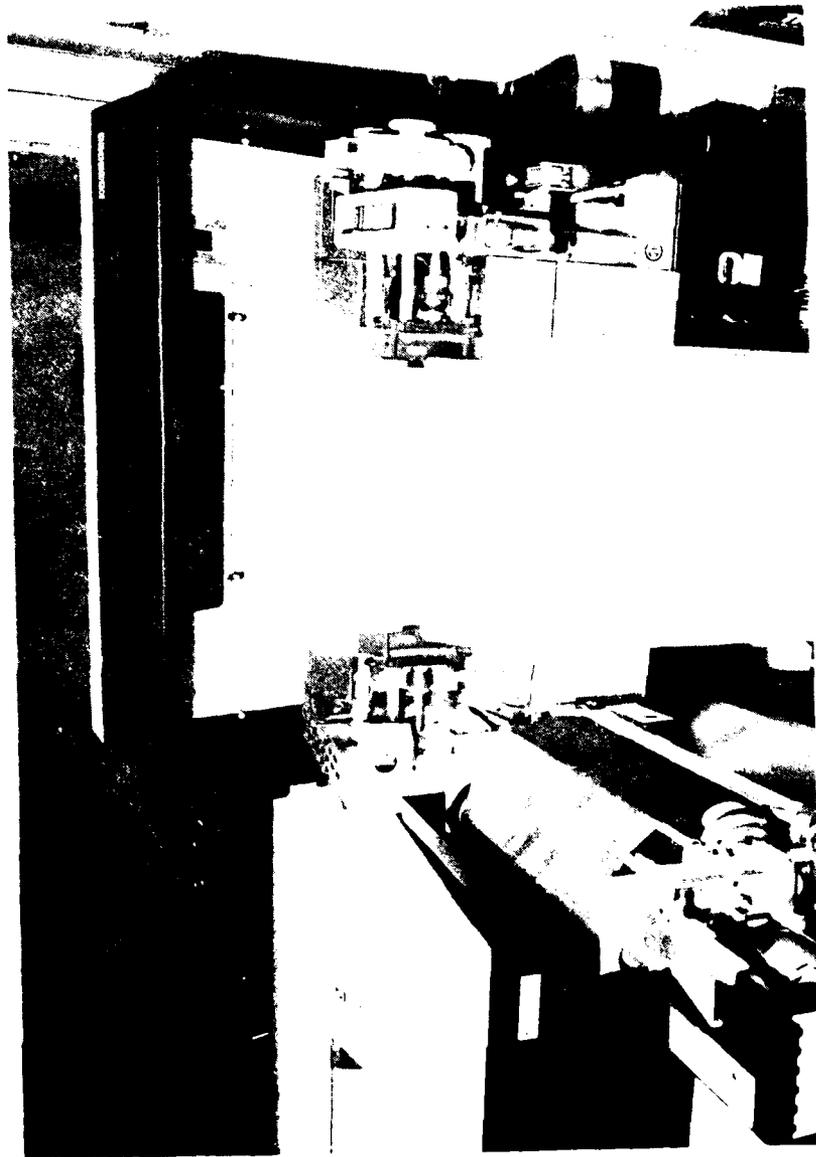


Figure 4-4. LPII-VA Line Printer

4.4.7.3 Troubleshooting

Troubleshooting the LP11 is accomplished by the self-test results and the diagnostic results. Adjustment procedures are given in the maintenance manual.

4.4.8 LA36 DECwriter II Printer Terminal

The LA36 DECwriter is a 96 character, 132 character width teleprinter. Print speed at 300 baud is 30 characters/second throughput at 10 characters/inch.

4.4.8.1 Preventive Maintenance

Inspection of the LA36 should include periodic checks for paper positioning, ribbon depletion, and carriage cleanliness.

4.4.8.2 Diagnostic Description

The diagnostic CZLACE0 (ZLAC) - LA36 Terminal- can be used to exercise the LA36. This diagnostic checks the console terminal interface logic, control logic, and echo.

4.4.8.3 Troubleshooting

The LA36 maintenance manual contains troubleshooting charts that are classified according to the available terminal options. The charts list symptom, problem area, cause, and references. This information should be used in conjunction with the diagnostic results.

4.4.9 SU 1652M Dual Monitor Display

The 1652 shown in Figure 4-5 is a 15-inch dual monitor display system with full-up memory for graphic displays, down-line loading capabilities, light pen, 60 function keys, and interactive graphics. An Intel 8080 microprocessor provides computational capability.

4.4.9.1 Preventive Maintenance

Preventive maintenance of the 1652 is minimal. Periodic checks should ensure that the blower is operating and the air filter is clean. DC power supply voltages should be checked to verify that the voltages

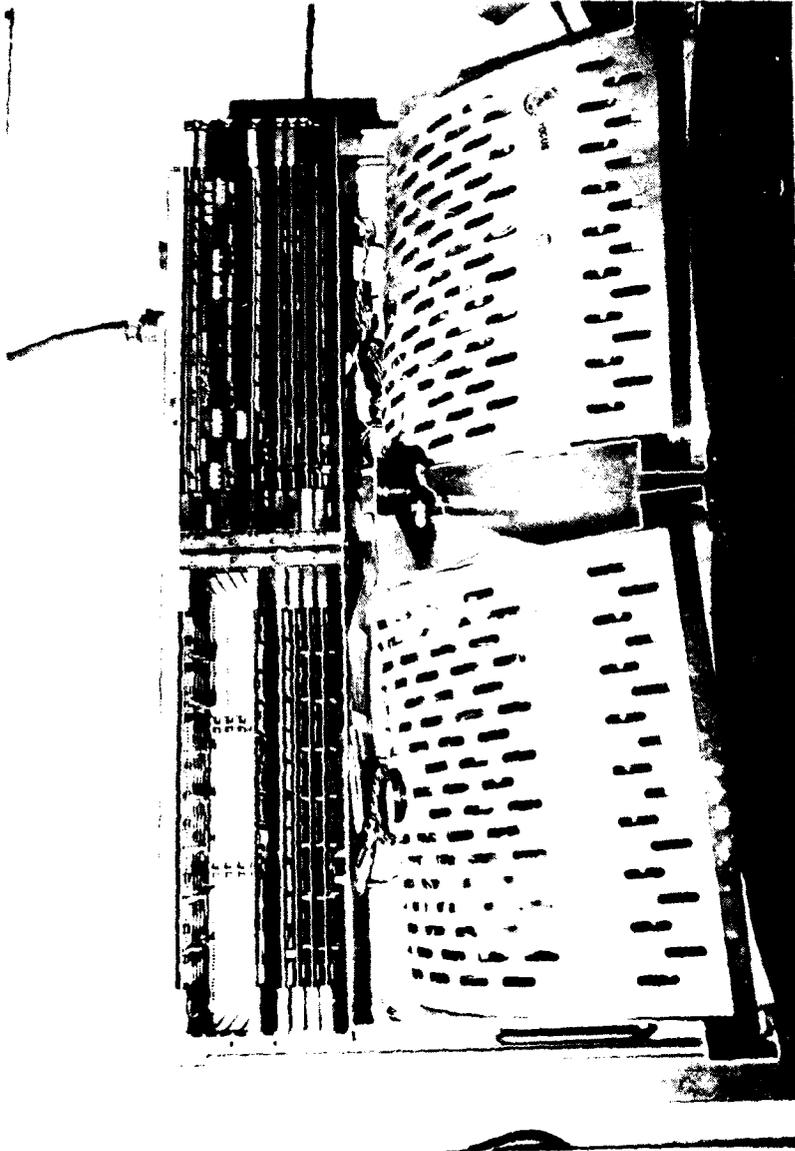


Figure 4-5. Top View Of SU-I652 M (cover removed)

are within tolerance. The console lights can be verified as operational by way of the console light test switch. Depressing the test switch activates all console lights which can then be inspected for failure.

4.4.9.2 Diagnostic Descriptions

Diagnostic micro-code can be down-loaded into the 1652 via the Program Load Module (PLM). This diagnostic micro-code (also known as maintenance micro-code) tests all aspects of the terminals hardware such as interrupts, display graphics, interactive graphics, light pen, keyboard, and overlay keyboards.

4.4.9.3 Troubleshooting

Troubleshooting the 1652 is accomplished using the fault isolation procedures flowcharted in the 1652 technical manual. The flowcharts isolate the fault to a replaceable module (printed circuit board). At this point, board swapping can be used to verify that the fault is on the isolated board.

4.4.10 Imlac PDS-4/L Graphic Display Terminal

Imlac's PDS-4/L is a 21 inch refresh type graphics display monitor that has 2048 x 2048 resolution and a 16 bit minicomputer which, along with the Pertec disk drive, form a stand-alone system.

4.4.10.1 Preventive Maintenance

The PDS-4/L has minimal preventive maintenance. Periodic checks should verify that the fans are operational, air filters are clean, panel lights are operational, and DC supply voltages are within tolerance.

4.4.10.2 Diagnostic Descriptions

The PDS-4/L is supplied with several diagnostic aids all of which help to isolate a malfunction to a particular printed circuit board (see Figure 4-6). The diagnostics are also used to aid various adjustment procedures performed on the graphic display. For example, the resistor settings in the DACs can be adjusted with the aid of a displayed test pattern containing many vectors arranged in a manner that makes the vector

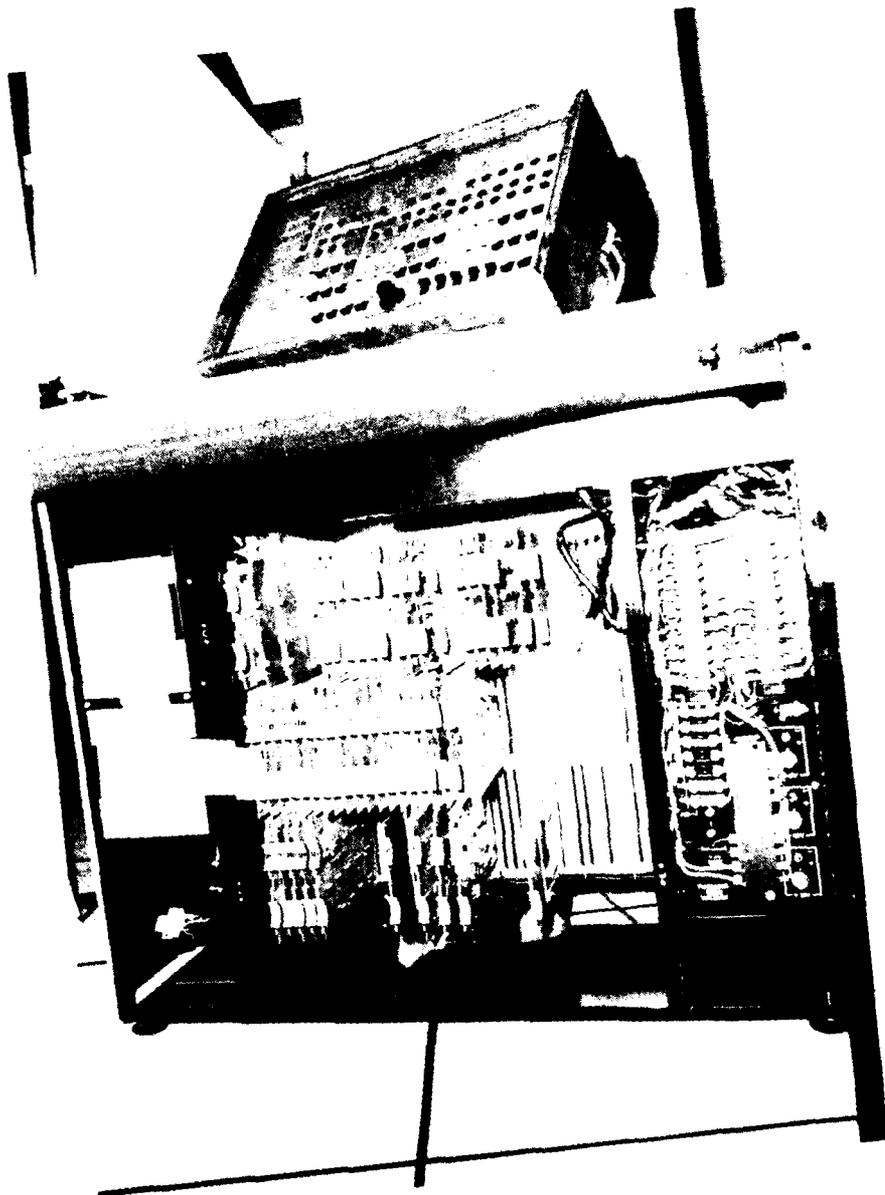


Figure 4-6. Imlac Minicomputer PC Boards

display sensitive to DAC adjustment. TTAPE3 listed below contains this adjustment pattern and several others. The diagnostics are given below.

- ROMLOD - ROM Test Program: This program tests the PDS-4/L read only memories (ROMs). Different machine configurations have different ROMs. The user defines the particular ROM to be tested. ROMLOD writes the selected ROM into memory, reads the memory locations in which the ROM was written, compares the results, then indicates the presents or absence of errors. The TOAS Facility PDS-4/L supports ROM 51 TTY-1 standard format.
- TMEM - Memory Test Program: The program tests the PDS-4/L for memory addressing errors, memory data integrity, and code execution reliability.
- TTAPE1 - Hardware Option Tests: TTAPE1 contains four main parts that test the options given below.
 1. TACI - Programmable real time clock option (referred to as the ACI or timer) test
 2. CIST - TKA and EIA variable baud rate (communications interface speed) test
 3. TCIRC - Circle/arc generator test
 4. TCOLOR - Color display alignment test
- TTAPE2 - Peripherals, Interrupts, and Display Functions Test: TTAPE2 contains three main parts shown below.
 1. SPIT - Interrupt tests include keyboard, TTY send/receive, TKA send/receive, 40 cycle sync, and end of display frame interrupts
 2. ABC - Plotting, Blink, and Variable Intensity Control (VIC) tests
 3. QUAD - The Monitor Control Interface (MCI), up to four keyboards, TTY, and TKA interfaces are tested

- TTAPE3 - Vector Generation and Display Test: Vector generation, and display capability tests include graphic displays that are used in digital to analog (D/A), and display alignment procedures. Eight tests are menued and given below.
 1. X-Axis Static Bit Pattern
 2. Y-Axis Static Bit Pattern
 3. X-Axis Suppression Grid Adjustment Pattern
 4. Y-Axis Suppression Grid Adjustment Pattern
 5. Long Vector Test
 6. Medium Vector Test
 7. Pedestal Adjustment Medium Vector Pattern
 8. Pedestal Adjustment Medium Vector Pattern

- TTAPE4 - Display Accumulator Test: The five tests shown below check the display accumulator operation.
 1. DADRE - Arithmetic operations test
 2. ARROYO- Rotate, reflect, and blink instruction tests
 3. STP - Stackpointer operation test
 4. CHOMP- Byte mode (legal byte instruction) test
 5. DDT - The Display Program Counter (DPC) and the eight Display Temporary (DT) registers are tested

Six subtests in STP test the Stackpointer (SP) register for loading/reading, POP, PUSH, and PUSHA instructions; and communication between the Program Counter (PC) and SP. The three subtests of DDT test the DPC for loading and POP/PUSH instruction errors.

- TTAPE5 - Peripherals, Display Block, and Register Test Program: TTAPE5 contains display block, keyboard, and increment/decrement tests shown below.
 1. TDSTB - Display set block test
 2. TKBD, TKBD2 - Keyboard diagnostic test for 67 or 92 key keyboards
 3. INDEC - Auto-increment and auto-decrement register test

- TTAP11 - Display Processing Unit (DPU)
Features and Modes Test: TTAP11 tests the basic DPU instructions shown below.

1. TFLAGS - Display and Synchronize Flags
2. TINTRP - Display and Synchronize Interrupts
3. TDCAM - Standard Cam Mode
4. TWAM - Word Address Mode (WAM)
5. TDROR - Rotation and Reflection
6. TMC14 - Monitor Control Interface (MCI)
7. T32K - Display test with memory over 32K
8. TBANKS - Test both memory banks
9. T8LDT - Display Subroutine Stack
10. TMC18 - New MCI Option command
11. TSCALE - Display Scale

4.4.10.3 Troubleshooting

When a malfunction occurs that does not have a well defined origin, verify the system as follows:

1. Check all system fuses
2. Check all system voltages
3. Run diagnostics

There are many functionally equivalent printed circuit boards in the PDS-4/L, such as accumulator boards, D/A converters, register boards (PC, MA, MB, DPC), display accumulators, and core memory boards. These boards can be swapped within the machine to determine if a malfunction changes. For example, the X-axis and Y-axis D/A converters are identical. If a problem is suspected within the X-axis D/A converter, it can be swapped with the Y-axis D/A converter. If the malfunction now occurs within the Y-axis D/A converter, the problem has been successfully isolated to the D/A converter originally in the X-axis D/A converter slot.

The PDS-4/L has fifty edge-connected removable printed circuit boards. Imlac supplies extensive troubleshooting charts in the PDS-4/L maintenance manual that attempts to isolate the malfunction to a particular circuit board.

The chart divides the PDS-4/L into five major areas: CPU, Communications, DPU and Graphic Options, Monitor, and Memory. Each area chart lists symptoms, possible causes, parts to investigate, and recommended diagnostic programs.

5. NEW COMPUTER TECHNOLOGY APPLICATIONS FOR THE TOAS FACILITY

The purpose of the TOAS facility is to provide the computer hardware and software environment to support experiments and demonstrations of computer technology as applied to the area of tactical intelligence processing. The overall Project 2315 goal is to improve all facets of the tactical intelligence process through automation of selected functional tasks.

The lack of state-of-the-art technology in the currently available TOAS Facility computer hardware and software constrains new approaches to solving tactical intelligence automation problems. Although the Facility has an extremely powerful mini-computer system (two PDP-11/70 computers and peripherals), experiments and technology demonstrations are necessarily limited by existing applications software and hardware constraints. The purpose of this section is to provide the Project community with some insight into other commercially available technology that could be used to support Project 2315.

5.1 MAGNETIC BUBBLE TECHNOLOGY

Magnetic bubble memory technology was first introduced by Bell Laboratories in 1967 and has now advanced to a stage of commercial production by several memory/computer manufacturers. Magnetic bubble memories can have an impact on the automated Tactical Air Intelligence System (TAIS) specifications for the 1990's; the TOAS Facility is the optimum environment for evaluating this new technology and possible applications.

This new technology should be evaluated against existing memory devices to determine the best device for the situation. Evaluation criteria include:

- Reliability
- Access Speed
- Ruggedness/Environmental Requirements

- Size
- Volatility
- Cost

Bubble memories are commercially available that are compatible with the current TOAS hardware configuration. The following paragraphs explain the theory and implementation of magnetic bubble technology as it is used as a random access storage device.

5.1.1 The Magnetic Bubble Memory Device

The heart of the magnetic bubble device is garnet crystal grown on a substrate (i.e. gadolimiun-gallium-garnet). This forms a single crystal, ferromagnetic thin film that allows propogation of distinct magnetic fields within the film. When a magnetic field is applied perpendicularly to the thin film, magnetic domains or "bubbles" are formed. As the intensity of the field is increased, the "bubble" gets increasingly smaller and eventually disappears.

The bubbles can be independently created and moved in a predictable pattern within the thin film. This characteristic allows bubble technology to be used as a non-volatile, random access storage medium. Bubbles have a nominal diameter of 3 microinches; a 10mm square chip can contain approximately 300k bubbles and is used as a 256k bit memory device. Figure 5-1 is a typical magnetic bubble device.

5.1.2 Transferring Magnetic Bubbles

In order to reduce the number of read/write devices required per chip, magnetic bubble memory technology has devised a method to move the the bubbles within a set pattern. This capability allows each data bit to be read/copied (magnetic bubble read is destructive), deleted, or re-generated. Bubble movement is accomplished by overlaying a fine pattern of soft ferromagnetic material on the thin garnet film and applying a rotating magnetic field parallel to the pattern surface. Bubble movement is in the direction of magnetic field rotation. The rotating magnetic

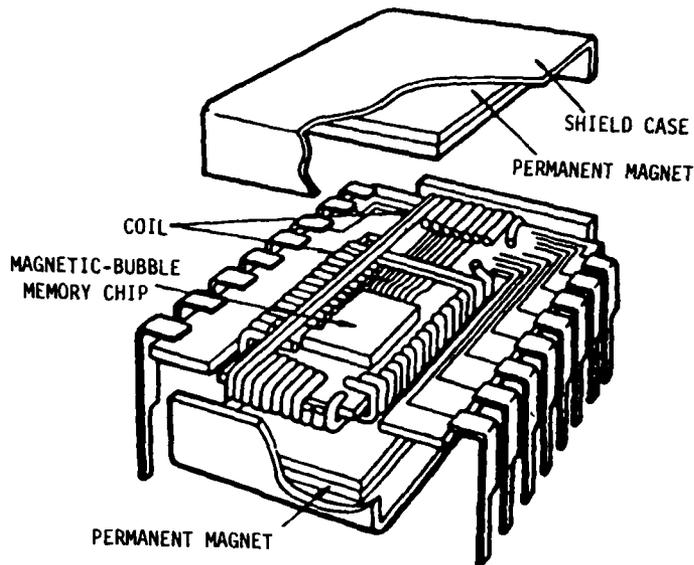


Figure 5-1. Typical Magnetic Bubble Device

field is produced by two mutually perpendicular solenoids covering the chip. The solenoids are fed with triangle-waveform currents, one lagging the other by 90 degrees in phase.

5.1.3 Data Writing/Reading Process

In order to employ magnetic bubble technology as a storage medium, bit patterns must be able to be generated, detected, and deleted in order to accomplish the functions of reading and writing. These activities are accomplished by generators, detectors, and transfer gates.

5.1.3.1 Generating Magnetic Bubbles

A non-magnetic conductor pattern is arranged between the thin garnet film and the ferromagnetic pattern. When a pulse current is passed through this pattern, a magnetic bubble is produced because the ferromagnetic pattern serves as a single winding coil to generate a magnetic field opposed to the bias field of the pulse current. The generated bubble is transferred along the path and the process is repeated to form bit patterns.

5.1.3.2 Detecting the Presense of Magnetic Bubbles

Normally the presense of a magnetic bubble indicates a "1" bit and the absense of the bubble a "0" bit. During the detect or read cycle the bit pattern is duplicated in order to reload memory concurrently with a "destructive" read operation. Bit patterns are detected by measuring the ammount of electricial resistance present under a bit detector.

5.1.3.3 Deleting Stored Magnetic Bubbles

Removing magnetic bubbles from the bit pattern is accomplished by applying a pulse current to inhibit the transfer of a particular bubble along the normal path. Bubbles, in a sense, are picked off the loop and directed to the ever present bit bucket.

5.1.4 Bubble Pattern Organization

There are two major bubble pattern organizations: serial loop and major-minor loop.

5.1.4.1 Serial Loop Organization

As the name implies, magnetic bubbles are stored in a single transfer path (see Figure 5-2). Data are serially transfered in the loop to point A where the datum is duplicated and transfered to the reading mechanism. The duplicate bubble continues to point C where it is removed or allowed to continue to travel along the serial loop memory pattern.

One of the draw backs of this type of architecture is the relatively long access times propogated by the distance the datum cell must travel before a read or write can be accomplished. This type of organization can be controlled by simple interface circuits and can be used for data loggers and other process control applications.

5.1.4.2 Major-Minor Loop Organizations

This type of storage system uses two different types of loops. The data are stored in a series of independent minor loops; reading/writing is accomplished by transferring the data from the minor loops to the major

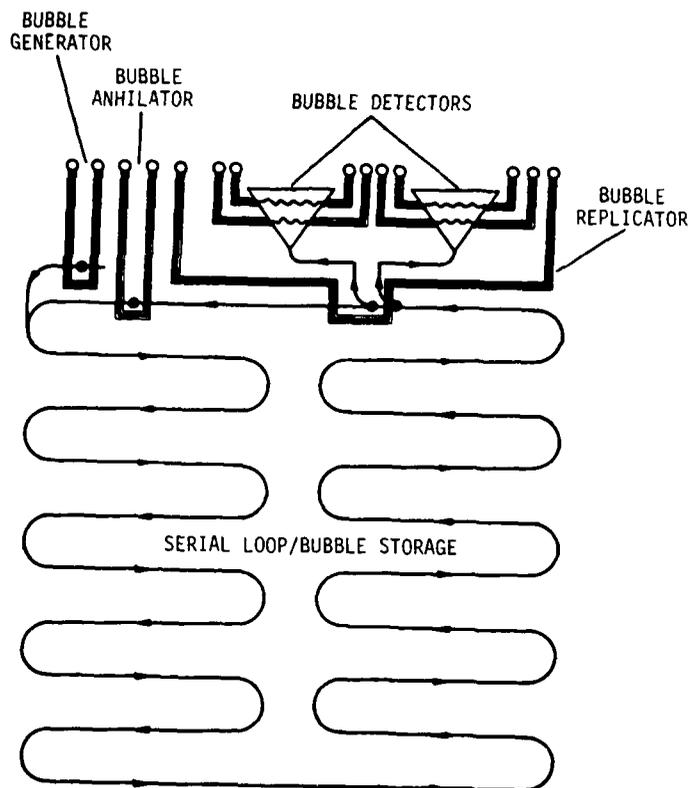


Figure 5-2. Serial Loop Bubble Organization

loop. The method of implementing bubble transfer determine the types of major-minor magnetic bubble loop architecture. The three major methods are:

- Transfer Gate System
- Block Replicator Transfer System
- Block Replicator Swap System

5.1.4.2.1 Transfer Gate System

Data stored in the minor loop pattern is transferred to the major loop pattern where it is duplicated and passed to the reading mechanism. The twin bubble continues along the major loop pattern to the anhilator

where it is removed from the loop or allowed to continue along the path to its appropriate minor loop for storage. If a new datum is required in that position, the old data is removed at the annihilator and a new bubble (logical "one") is generated prior to storage in the minor loop. Refer to Figure 5-3.

5.1.4.2.2 Block Replicator Transfer System

This method uses two distinct major lines; one for the read operation and one for the write operation. The write operation is accomplished by reading the datum stored in the minor loop. This effectively removes the old data from the minor loop. Concurrently, the bubble generators write the new information onto the major write line. When the empty cell in the minor loop and the new information in the write major loop are aligned at the transfer gate, the information is stored on the minor loop. The read operation duplicates the datum and transfers the duplicate to the read major line for sensing. The original is still stored on the minor loop. Refer to Figure 5-3.

5.1.4.2.3 Block Replicator Swap System

This method is very similar to the block replicator transfer system. The read operation is essentially the same. During the write operation, old data does not have to be removed from the minor loop prior to writing new data. This is possible because the old and new data exchange places. The new data on the minor loop is now stored while the old data on the major write loop is swept away to the bit bucket. Refer to Figure 5-3.

5.2 WINCHESTER DISK TECHNOLOGY

Disk drives have been used as the primary medium for low cost random access mass storage in all tactical intelligence computer applications. A variety of disk types and technologies are currently employed at fixed facility (e.g. Reconnaissance Technical Groups) and deployable systems (e.g. Intelligence Information Support System) intelligence centers. Both the fixed facility and the deployable systems are currently evolving very complex data handling processes to handle an ever increasing amount of intelligence data. One factor that heavily influences system performance

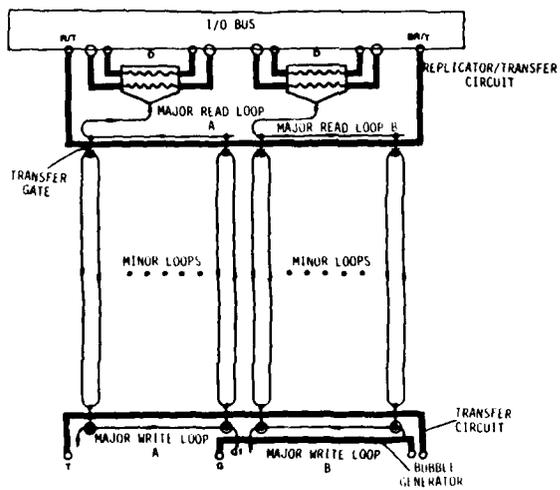
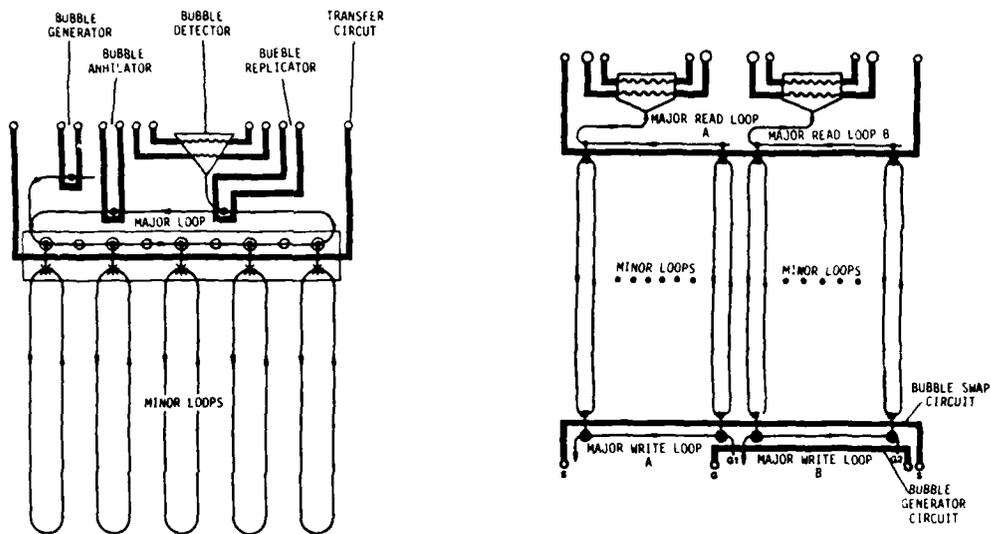


Figure 5-3. Major-Minor Loop Organization

(i.e. response time) is the mass storage (disk system) configuration and technology. This section provides an overview of one type of disk technology that has not been integrated into currently operational intelligence systems; the direct application and benefits to the intelligence function make Winchester disk technology a candidate for implementation and investigation at the TOAS Facility.

5.2.1 Winchester Drives

In 1973, IBM introduced the first Winchester type disk systems, the Model 3340. This technology has been rapidly expanded and improved by other manufacturers and Winchester disks are readily available from many commercial sources. A Winchester disk drive is characterized by:

- One or more 5, 8, or 14 inch rigid disk platters
- Fixed or movable read/write heads
- Recording mechanism and media in one package
- Sealed air recirculating system

The most distinguishing features of this type of disk system are the sealed air recirculating system and the integration of the disk platters and the recording assembly into a single unit. These characteristics reduce maintenance time and costs and promote more reliable operation in uncontrolled environments.

5.2.2 Winchester Recording Process

Winchester disk systems employ the same general recording methods and theory as other disk systems. The the unique characteristics of this technology are exploited to produce a system that is very reliable, compact, fast, and inexpensive.

A Winchester device is composed of one or more rigid aluminum disks that have been coated with a magnetic recording medium. This coating varies from manufacturer-to-manufacturer but is similar to the coating on removable disk type systems. Since the flying heads in some models actually "land" on a homing track, hardness in this area is sometimes a factor. As with most conventional systems, both sides of the disk platter are used for data

storage (except the bottom surface of the bottom platter which normally contains positioning data).

The data recording/reading process is accomplished by the sensing head. The head is composed of three aerodynamically shaped rails or ridges that literally fly on an air bearing of less than 30 microinches from the surface of the disk. The trailing edge of the middle ridge contains the actual read/write device which is a wire wound, ferrite core. Since the disks and head assemblies are hermetically sealed in one module which recirculates and filters air internally, the ferrite recording device can fly closer to the recording surface without head crashes due to contamination. New advances in the thin-film head technology will further improve the Winchester capacity.

5.2.3 Winchester Recording Limitations

As with any disk system, the number of bits of information that can be recorded is a function of the recording head and the disk media. The width of the center rail of a Winchester head is limited by a problem of durability. A thin rail allows increased data storage at the risk of high failure rate due to the fragile head assembly. Approximately 1000 per inch have been achieved.

The number of bits per track is also limited by the disk platter and head design. The composition/magnetic properties of the disk surface limit the data density. In addition the magnetic properties of the ceramic head core (i.e. ferrite particles) can not respond to reversals of current flow in excess of 10 million per second. This limitation also affects the density of data recorded on the disk.

5.3 VIRTUAL PROCESSORS - VAX-11/750

The PDP-11/70 CPU has evolved into the standard computer in the intelligence community. For this reason, the TOAS baseline hardware configuration specified this computer for initial investigation work. As the Project matures and other data manipulation requirements are evolved, additional computational capabilities will be needed to support simul-

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taneous operation of several complex software systems. This section provides information on DEC's newest 32 bit minicomputer, the VAX-11/750.

5.3.1 VAX-11/750 Capabilities

The VAX-11/750 is a 32 bit virtual processor that has been priced to be comparable to the PDP-11/70. The 11/750 software and peripherals are compatible with the more powerful 11/780; this compatibility supports easy migration to the more powerful CPU when required. The following characteristics make the VAX a more powerful computer than the PDP:

- 32 bit word length - allows 4 gigabytes (4,000,000,000) of virtual address space to be used without overlays,
- Semiconductor technology reduces physical size and power requirements,
- 32 or 64 bit floating point processing
- Sixteen 32-bit general purpose registers
- 4 Kbytes of cache memory, and
- 240 basic instructions, PDP 11 compatibility mode allows PDP 11 software to be executed.

5.3.2 VAX Software

The VAX Virtual Memory System (VMS) operating system supports several types of user environments (timesharing, multi-user, real time, or batch). These separate environment can be used independantly or simultaneously. VMS has an efficient scheduler, paging algorithm, and file processing capabilities. VMS supports the following higher level languages/utilities that are of interest to the intelligence community:

- COBOL
- Fortran IV
- Pascal
- Basic
- PL1

- DECnet
- File editors
- Symbolic debuggers

5.4 A RELATIONAL DATA MANAGEMENT SYSTEM - ORACLE

The traditional method of building and using data bases employs hierarchical and/or network data structures and data management application programs for information processing. Another method of solving the data management problem uses the relational data base concept. Relational data base systems have been proposed, developed, and used for many years with varying degrees of success. This section provides an introduction to Oracle, a relational data base management system which is a candidate for implementation at the TOAS Facility.

Oracle is a highly successful implementation of the relational approach to data base management. This software, developed by Relational Software Incorporated and has been field tested for over a year with excellent results. Users have rated Oracle performance to be better than the more traditional hierarchical and network data structure languages (e.g. Sarp V, Gim II, Adabas, and DBMS-11). Oracle is currently available for implementation on PDP-11/70 computer equipment.

5.4.1 Oracle Data Language

Oracle uses a high-level relational data language, Sequel 2 to perform the data management functions of query, data manipulation, definition, and control. Sequel 2 was developed by IBM for implementation on their still-to-be-released version of a relational data base system and provides several levels of user complexity. This language provides all the necessary commands and functions for the all users (programmers, system managers, functional users). Sequel 2 capabilities include:

- Terminal language - an on-line terminal query and update capability for the functional user,
- Programmer's sub-language - Sequel 2 statements can be embedded in procedural programming languages such as Cobol, Fortran, Pl-1, "C", or assembly language,

- Report Generation - Orator is the report writer that can format and print information from the data base, and
- Data Definition and Control - used to define the data items and tables in the data dictionary.

5.4.2 Oracle Integrated Data Dictionary

The on-line data dictionary provides a tool assisting users in effectively planning, controlling and evaluating the current data structure. The dictionary defines all data items and tables (relations) found in the data base. The data dictionary provides:

- Data Definition - permits dynamic definition and expansion of data items and relations,
- Data Normalization - presents highly complex data relations as a collection of independent relations,
- Dictionary Query - the data attributes are readily available and can be searched via queries, and
- User Sub-schema - each user can have a logical view of the data base.

5.4.3 Oracle Performance Characteristics

Oracle has the performance characteristics to provide the data base management services to support R&D investigations in support of Project 2315

- PDP 11-70 - can be implemented on the standard intelligence community hardware; compatible with TOAS hardware,
- Multi-thread - can support simultaneous data access by many users and/or batch processes,
- Data Compression - data items are stored in a compressed form, no space is reserved for missing items,
- Compressed Indexes - any data item can be indexed by an inverted file, files are compressed to conserve memory and disk space, and
- Multiple Data Base Support - Oracle can support simultaneous activity on separate data bases; Oracle code is re-entrant.

5.5 OTHER FACILITY SOFTWARE

Two software programs were supplied to the TOAS Facility during this year: Program Load Module and SU 1652 to DL11-E Interface.

5.5.1 Program Load Module

The Program Load Module (PLM) is a down-line loader for the SU 1652 terminal. This software was developed by Sperry Univac Corporation for the Rome Air Development Center. A copy of the object software was provided for use at the TOAS facility by the government. The PLM software allows the user to easily update tables containing SU 1652 micro-code modules and terminal characteristics. This allows system managers to dynamically change the software characteristics of SU 1652 terminals. Complete documentation is provided at the TOAS Facility.

5.5.2 SU 1652 to DL-11E Interface

This software was developed by OSI under contract to the Rome Air Development Center and provided to the TOAS Facility. The modules have not been implemented.

This software was intended to provide an inexpensive alternative for interfacing the SU 1652 terminal to the PDP-11/70. By using the SU 1652 asynchronous mode, site requiring a small number of SU 1652 terminals can avoid the cost of a BR 1569/1566 multiplexer and use the DL-11E interface cards. This software will be investigated/implemented next year.

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GLOSSARY

Access	Seeking, reading, or writing data on a storage device
Access method	Techniques for locating data (e.g. serial access, random access, remote access, virtual sequential access method (VSAM), hierarchial indexed sequential access method (HISAM))
Access time	The time that elapses between an instruction being given to access data and that data being available for use
Address	An identification (number, name, label) for a location in which data is stored
ADP	Automated Data Processing
Algorithm	A computational procedure or technique
AM	Amplitude modulation
Amplitude Modulation	Method of signal transmission in which the amplitude of the sine wave carrier signal is changed in accordance with the information to be transmitted
Analog signal	A signal that has the form of a continuously varying physical quantity, i.e., voltage
ASCII	American Standard Code for Information Interchange - an eight level code
ASR	Automatic Send-Receive teletypewriter machine
Assemble	To convert a routine coded in a higher level computer language into actual machine language instructions
Associative storage	Storage which is addressed by content rather than by location
Asynchronous transmission	Start-stop transmission; transmission in which each information character (word or block) is individually synchronized by use of a start and stop elements
Attribute	A field containing information about an entity

Baud	Unit of signaling speed; normally the same as bits per second
Baudot	Five bit, 32 character code used by some TTY transmission systems
BCD	Binary Coded Decimal - a six bit alphanumeric code
Binary code	An electrical representation of information expressed in the base two number system
Binary search	A method for searching a sequential file/table; procedure is based on algorithm that divides data into two equal groups and determines which group contains the required data and then repeats procedure with that group
Bit	A contraction of the words "binary digit" - smallest amount of information that can be represented (normally thought of as a one or zero)
Blocking	Combining two or more records so that they are jointly read or written by one machine instruction
BPS	Bits per second
bpi	Bits per inch
BR-1566	Massbus controller used to interface the BR-1569 to the PDP-11/70
BR-1569	Communications multiplexer that supports 8-32 channels- manufactured by Bunker Ramo - part of baseline configuration
Byte	A group of data handled as a unit (commonly 8 bits is to one byte)
Cache memory	High speed memory placed between slower main memory and the processor; cache increases effective memory transfer rate
CATIS	Computer Aided Tactical Information System
chaff	Small, light scraps of paper tape
chip	The substrate on which LSI circuits are fabricated; sometimes referred to as the circuits themselves
Circular buffer	A queue that has front and rear pointers to keep track of information in a defined area

Circular file	An organization for a file of high volatility, in which new records being added replace the oldest records
CODASYL	Conference of Data Description Languages; DBMS type
Concatenate	To link together - a concatenated data set is a collection of logically connected data sets
Control character	A character whose occurrence initiates, modifies, or stops an on-going operation
CPU	Control Processing Unit
Cylinder	A concept of storage using magnetic disks - a area read without moving the arms of the disk drive
DASD	Direct Access Storage Device
Data	Numbers, text, fact, information which are represented in a formal structure so that it can be processed by computers
Data administrator	An individual with an overview of an organizations data base
Data base	A collection of interrelated data stored together to serve one or more applications
Data base management system	The collection of software required for using the data base
Data dictionary	A catalogue of all data types giving their names and structures
Data structure	Well defined format and access conventions associated with a particular class of information
Db, db	Decibel
DBCS	Data Base Control System
DBMS	Data Base Management System
DCL	DEC Command Language
DCL	Device Control Logic
DEC	Digital Equipment Corporation
Decibel	A unit for measuring relative strength of a signal parameter such as power, voltage etc

DEC/X-11	A configurable system exerciser diagnostic program in the MAINDEC-11 diagnostic package
DDL	Data Definition Language
Demodulation	The process of retrieving data from a modulated carrier signal - the opposite of modulation
Diagnostic	A program that tests logic and reports any faults it detects
Direct access	Retrieval or storage of data by a reference to its location on a volume, rather than relative to the previously retrieved or stored data
DL 11E	Single line asynchronous interface manufactured by DEC
DMA	Direct Memory Access
DPU	Display Processing Unit
DVM	Digital Volt Meter
EBCDIC	Extended Binal Coded Decimal Interchange Code; an eight bit alpha-numeric code
ECC	Error Correction Code
EDP	Electronic Data Processing
EIA	Electronics Industry Association
EIA Interface	A standard set of signal characteristics (time duration, voltage, and current) specified by the Electronic Industries Association
Error-correcting Code	A code having a sufficient number of signal elements to allow error detecting and/or correcting at the receiving station
Even parity	A check (or count) of a block of data to insure that an even number of bits are contained in the block
Fatal Error	An error in a system or program that inhibits any further system operation or program execution
FDM	Frequency Division Multiplex
FDX	Full Duplex

Fiber Optic Waveguides	Filaments of glass through which a light is transmitted for long distances by means of internal reflections
Field	A set of contiguous bytes in a record
FM	Frequency Modulation
FPP	Floating Point Processor
Frequency	The rate at which a current alternates
Frequency division multiplex	multiplex system in which the available transmission frequency range is divided into narrower bands
Frequency modulation	Method of modifying the frequency of the sine wave carrier to support information transmission
Full Duplex	Equipment capable of transmission simultaneously in two directions
Gate	A basic logic circuit
Half Duplex	A circuit that can transmit information in both directions, but not simultaneously
Hamming Code	A error correcting/detecting code using redundant bits
Hertz	A unit of frequency measurement, i.e., one hertz equals one cycle per second
HD	Half Duplex
Hollerith code	A alphanumeric code used in card readers and sorters
Hz	Hertz
IAS	Interactive Applications System
IC	Integrated Circuit
Index	A table used to determine the location of a record
Intelligent terminal	A terminal that can perform data processing/manipulation tasks without relying on the host computer
Interface	The boundary between two pieces of equipment: consists of physical characteristics, signal strengths, information codes, protocols etc
Interleaved	Assigning consecutive physical memory addresses alternately between two memory controllers

Inverted file	A file structure which permits fast spontaneous searching for previous unspecified information - independant lists or indices are maintained in records keys which are accessable according to the values of specific fields
I/O	Input/Output - refers to computer generated information displays and input
I/O channel	An equipment that forms part of the input/output system
ips	Inches per second
KSR	Keyboard Send Receive teletype machine
LA-36	30 characters per second dot maxtrix printer commonly used as a console device
Label	A set of symbols used to identify an item, record, message or file
LED	Light Emitting Diode
Link	The process of connecting object modules into a contiguous executable task
List	An ordered set of data items, a chain
Logical	Data organization, hardware, or system that is perceived by the applications programer, different from real (physical) form
Longitudinal redundancy check	A method of checking the reliability of a block of data
LRC	Longitudinal Redundancy Check
LSI	Large Scale Integration; method of placing many electronic circuits on one small chip
MAINDEC-11	A system diagnostic package containing the XXDP monitor and system component diagnostics.
MASSBUS	36 bit wide data path between the CPU, memory and high speed peripherals
MDLI	Minimum Device Level Interface
Mbyte, MB	Mega-byte; 1,000,000 bytes

Mean time to failure	The average length of time for which the system or component works without failing
Mean time to repair	Average time required to repair the system or component
MHz	Megahertz - a unit of frequency measurement equal to one million hertz
mil	Measurement of thickness; 0.001 inch
MODEM	Modulator-Demodulator; a device that can modulate a signal for transmission and demodulate for reception
Modulation	A process of changing the characteristics of the carrier signal to reflect the values of the transmitted data
MOS	Metal Oxide Semiconductor; a type of LSI chip
MPG	Maintenance Program Generator
MSI	Medium Scale Integration; solid state technology with fewer circuits per chip than LSI
MTTF	Mean time to failure
MTTR	Mean time to repair
Multi-access	The ability to allow several users simultaneous access to the computer
Multiplex	Using a common channel to support more than one process or user by dividing the frequency band into narrower bands (FDM) or using time slots (TDM)
Multiplexer	A device that enables more than one signal to be sent simultaneously over one physical circuit
Multiprogramming	The method which supports several independent jobs processed together to maximize system performance
Multi-thread	The ability of a process (normally a data base management system) to support more than one user accessing a file or portion of code
MUSDAB	Multi-Source Data Base - Advanced R&D data base/effort to support Project 2315
Node	A point of junction between links - a switching or processing center

On-line	A device that is connected directly to the computer; normally thought of as an interactive device
Parity check	The process of adding non-information bits to a block of data to make the total number of bits even or odd
PDP 11/70	Programable Digital Processor; the 11/70 is the most powerful 16 bit minicomputer in the DEC 11 series family of processors; part of TOAS baseline configuration
PDS-4/L	Stand-alone graphic refresh CRT terminal - part of baseline configuration; manufactured by Imlac
Peripheral device	Input or output devices of a computer (i.e. printers, magnetic tape drives, disks, consoles, CRTs, etc)
Peripheral interface	A standard interface between the computer and its peripherals designed to accomodate changes
PMI	Preventive Maintenance Inspection
Protocol	A fixed procedure required to initiate and maintain a communications process
RADC	Rome Air Development Center, Griffiss AFB, NY
RAM	Random Access Memory
Random access	The ability to access data directly without searching through other extraneous data
Real time	A process or transmission which occurs sufficiently fast that it is used in essentially the same manner as if it were instantaneous
Redundancy check	An automatic or programmed check based on characters used especially for checking purposes
Response time	The time the system takes to react to a given command or execute a particular process
RH-70	Massbuss controller for high speed peripherals
RF	Radio Frequency
RFI	Radio Frequency Interference
RO	Receive Only
ROM	Read Only Memory

RP06	A dual access moving head disk system; each pack can store 176 MB; part of TOAS baseline configuration
RS-232 Interface	An EIA standard for interfacing terminals and computer equipment
Seek	The mechanical movement of the flying head involved in locating a record on a random access device
Semaphore	A mechanism for synchronizing a set of processes; used to preclude one process from changing data (or code) being used by another process
Serial	An interface in which the bits of data are transmitted or processed one at a time
Simplex circuit	A circuit that allows transmission in a single direction only
Soft copy	A temporary record - normally associated with a CRT display unit
SPC	Small Peripheral Controller
Stop bit	The signal characteristic that denotes end of transmission
SU-1652	A dual screened CRT developed by Sperry Univac and used in the automated intelligence community
Synchronous	Having a constant time interval between successive bits, characters, or events
Task	A linked group of object modules ready for execution
TDM	Time Division Multiplex
TDMA	Time Division Multiplex Access
Teletype	Trademark of the Teletype Corporation that produces tape punches, page printers, etc used for communications systems
Throughput	The total amount of useful information processed during a specified interval
Time division multiple access	Physically separated devices are allowed access to a single device by allocating time slots to each one

TOAS	Tactical Operations Analysis Support Facility - the RADC test and demonstration facility at Langley AFB, Virginia
TTY	Teletype
UIC	User Identification Code
UFD	User File Description
UNIBUS	18 bit data path connecting all DEC peripheral devices to the 11/70 CPU
Virtual	Adjective implying that something in reality is different than it appears to a set of programs or users
Virtual storage	A technique that allows users to employ a computer as though it has a much larger memory than its real memory capacity
VRC	Vertical Redundancy Check
Word	A sequence of bits or characters treated as a unit; two bytes (16 bits) is one DEC 11/70 word
WPM	Words per minute
Xerox 1750	45 CPS letter quality daisy wheel printer - part of TOAS baseline configuration
XXDP	The "catch-all" name for the diagnostic programs contained in the MAINDEC-11 diagnostic package

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